Please type a plus sign (+) inside this box → [+]

PTO/SB/21 (08-00)
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U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	10/020,741
Filing Date	December 12, 2001
First Named Inventor	Dennison et al.
Group Art Unit	2813
Examiner Name	T. Nguyen
Attorney Docket Number	2269-3259.1US (91-0473.02/RE)

ENCLOSURES *(check all that apply)*

- [x] Postcard receipt acknowledgment (attached to the front of this transmittal)
- [x] Duplicate copy of this transmittal sheet in the event that additional filing fees are required under 37 C.F.R. § 1.16
- [ ] Preliminary Amendment
- [ ] Response to Restriction Requirement/Election of Species Requirement dated
- [x] Response to Action Under *Ex Parte Quayle* dated January 10, 2005 Including Petition Under 37 C.F.R. 1.183 to Suspend or Waive the Rules
- [ ] Additional claims fee - Check No. in the amount of $
- [ ] Letter to Chief Draftsman and copy of FIGS. with changes made in red
- [ ] Transmittal of Formal Drawings
- [ ] Formal Drawings (sheets)
- [ ] Information Disclosure Statement, PTO/SB/08A (08-00); [ ] copy of cited references
- [ ] Supplemental Information Disclosure Statement; PTO/SB/08A (08-00); copy of cited references and Check No. in the amount of $180.00
- [ ] Associate Power of Attorney
- [x] Petition for Extension of Time and Check No. 7859 in the amount of $1,020
- [ ] Petition
- [ ] Certified Copy of Priority Document(s)
- [ ] Assignment Papers *(for an Application)*
- [ ] Terminal Disclaimer
- [ ] Terminal Disclaimer
- [ ] Terminal Disclaimer
- [x] Other Enclosure(s) *(please identify below)*:

  Check in the amount of $130.00
  Declaration by Joseph A. Walkowski Regarding Refusal of Charles H. Dennison to execute Supplemental Declaration with attached Exhibits A-F
  Request for Transfer of Surrendered Original Patent
  Executed Supplemental Reissue Declaration

Remarks

The Commissioner is authorized to charge any additional fees required but not submitted with any document or request requiring fee payment under 37 C.F.R. §§ 1.16 and 1.17 to Deposit Account 20-1469 during pendency of this application.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm *or* Individual name	Joseph A. Walkowski	Registration No. 28,765
Signature		
Date	May 26, 2005	

CERTIFICATE OF MAILING

Express Mail Label Number: EL994822930US

Date of Deposit: May 26, 2005

Person Making Deposit: Steve Wong

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Dennison et al.

Serial No.: 10/020,741

Filed: December 12, 2001

For: OPTIMIZED CONTAINER STACKED CAPACITOR DRAM CELL UTILIZING SACRIFICIAL OXIDE DEPOSITION AND CHEMICAL MECHANICAL POLISHING

Confirmation No.: 2283

Examiner: T. Nguyen

Group Art Unit: 2813

Attorney Docket No.: 2269-3259.1US
(91-0473.02/RE)

NOTICE OF EXPRESS MAILING

Express Mail Mailing Label Number: EL994822930US

Date of Deposit with USPS: May 26, 2005

Person making Deposit: Steve Wong

RESPONSE TO ACTION UNDER *EX PARTE QUAYLE* INCLUDING PETITION UNDER 37 C.F.R. 1.183 TO SUSPEND OR WAIVE THE RULES

Mail Stop Amendment
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

This paper is submitted in response to an action under *Ex parte Quayle* mailed on January 10, 2005, the two-month shortened statutory period for response to which expired on March 10, 2005. This paper is submitted with a petition for a three month extension of time and the required fee.

Remarks begin on page 2.

REMARKS

The *Ex parte Quayle* Action mailed on January 10, 2005 has been received and reviewed. Claims 61 through 71 are currently pending in the application and have been allowed. The Office Action required in response thereto to secure allowance of the application:

1) filing of a supplemental reissue oath or declaration averring that all errors being corrected in the reissue application arose without any deceptive intention on the part of the applicants; and

2) surrender of original U.S. letters patent number 5,270,241.

Applicants submit herewith in response to the *Ex parte Quayle* Action:

1) Supplemental Reissue Declarations executed by inventor Michael A. Walker averring that every error in the patent being corrected in the present reissue application, and which is not covered by the prior oath and/or declaration, arose without any deceptive intention on the part of the applicants; and

2) Request for Transfer of Surrendered Original Patent. Original U.S. letters patent number 5,270,241 were previously surrendered on October 27, 2000 under Reissue Application No. 08/759,058, now US Patent No. RE38,049 E, issued March 25, 2003. A copy of the date-stamped return postcard is attached to the request evidencing receipt of the original letters patent. Applicants respectfully request that the previously surrendered originally patent be transferred from the abandoned reissue application to the present continuation reissue application.

The Outstanding Action pursuant to *Ex parte Quayle*

The Action pursuant to *Ex parte Quayle* required in response thereto to secure allowance of the application the filing of a supplemental reissue oath or declaration covering claims 61 through 71 averring that all errors being corrected in the reissue application arose without any deceptive intention on the part of the applicants.

Applicants submit herewith in response to the Action pursuant to *Ex parte Quayle*, a Supplemental Reissue Declaration executed by inventor Michael A. Walker averring that every error in the patent being corrected in the present reissue application, and which is not covered by

the prior oath and/or declaration, arose without any deceptive intention on the part of the applicants.

The inventor Charles H. Dennison has refused to sign the Supplemental Declaration, as evidenced by the accompanying DECLARATION OF JOSEPH A. WALKOWSKI REGARDING REFUSAL OF CHARLES H. DENNISON TO EXECUTE SUPPLEMENTAL REISSUE DECLARATION.

This paper is submitted in response to an Action pursuant to *Ex parte Quayle* mailed on April 6, 2005 by Examiner Tuan H. Nguyen. The relevant background facts are set forth below, as is a Petition to Suspend or Waive the Rules Pursuant to 37 C.F.R. 1.183.

Statement of Facts

Applicant's attorney forwarded a supplemental reissue declaration to Micron Technology, Inc. for execution by the inventor Michael A. Walker. Mr. Walker executed the Supplemental Reissue Declaration, the original of which is enclosed herewith.

Applicant's undersigned attorney knew that the inventor Charles H. Dennison had left the employ of Micron Technology, Inc. and now resides in San Jose, California in the employ of Ovonyx, Inc., a competitor with some product lines under development by the Assignee of the present application, Micron Technology, Inc.

To summarize the current situation, the inventor Charles H. Dennison was reached by email on April 1, 2005 with attachments including a supplemental reissue declaration, as set forth in more detail in the accompanying DECLARATION OF JOSEPH A. WALKOWSKI REGARDING REFUSAL OF CHARLES H. DENNISON TO EXECUTE SUPPLEMENTAL REISSUE DECLARATION.

On May 2, 2005, the undersigned followed up with Mr. Dennison by email, re-forwarding the prior email of April 1, 2005 and attachments thereto, and no response was received.

On May 16, 2005 the undersigned contacted Mr. Dennison by telephone at his place of business, Ovonyx, Inc. regarding whether Mr. Dennison had received the emails and attachments sent on April 1, 2005 and May 2, 2005 and whether he would sign the supplemental reissue declaration. Mr. Dennison, who is known personally to the undersigned, acknowledged receipt

of the emails and attachments and stated that he would not sign the supplemental reissue declaration.

Petition for Suspension or Waiver of the Rules Pursuant to 37 C.F.R. 1.183

Accordingly, Applicants herein respectfully petition for suspension or waiver of the rules pursuant to 37 C.F.R. 1.183, and specifically for a waiver of the requirement for a Supplemental Reissue Declaration executed by inventor Charles H. Dennison he has refused to execute and return to Applicants' attorney the Supplemental Reissue Declaration received by him on April 1, 2005 and May 2, 2005. Applicant also relies upon M.P.E.P. 1414.01 as authorizing the filing of this petition as an appropriate response in the present circumstances.

Applicants submit herewith in response to the Office Action pursuant to *Ex parte Quayle* of January 10, 2005:

1) DECLARATION OF JOSEPH A. WALKOWSKI REGARDING REFUSAL OF CHARLES H. DENNISON TO EXECUTE SUPPLEMENTAL REISSUE DECLARATION with attached Exhibits A through F;

2) REQUEST FOR TRANSFER OF SURRENDERED ORIGINAL PATENT;

3) a Supplemental Reissue Declaration executed by the inventor Michael A. Walker averring that every error in the patent being corrected in the present reissue application, and which is not covered by the prior oath and/or declaration, arose without any deceptive intention on the part of the applicants; and

4) The required fee under 37 C.F.R. 1.17(h) in support of the suspension or waiver of the rules pursuant to 37 C.F.R. 1.183.

The Office is hereby authorized to charge any additional fees required to Deposit Account No. 20-1469.

CONCLUSION

Applicants respectfully request prompt and favorable action, and issuance of a Notice of Allowability with an accompanying Notice of Allowance and Fee(s) Due. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully submitted,

Joseph A. Walkowski
Registration No. 28,765
Attorney for Applicants
TRASKBRITT
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

May 26, 2005
JAW/dlm:slm

Document in ProLaw

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Dennison et al.

Serial No.: 10/020,741

Filed: December 12, 2001

For: OPTIMIZED CONTAINER STACKED CAPACITOR DRAM CELL UTILIZING SACRIFICIAL OXIDE DEPOSITION AND CHEMICAL MECHANICAL POLISHING

Confirmation No.: 2283

Examiner: T. Nguyen

Group Art Unit: 2813

Attorney Docket No.: 2269-3259.1US
(91-0473.02/RE)

NOTICE OF EXPRESS MAILING

Express Mail Mailing Label Number: EL994822930US

Date of Deposit with USPS: May 26, 2005

Person making Deposit: Steve Wong

DECLARATION BY JOSEPH A. WALKOWSKI REGARDING REFUSAL OF CHARLES H. DENNISON TO EXECUTE SUPPLEMENTAL REISSUE DECLARATION

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

I am a shareholder and director of the law firm of TraskBritt, P.C., located at 230 South 500 East, Suite 300, Salt Lake City, Utah 84102, Reg. No. 28,765.

I am an attorney of record in the above-referenced application.

I know the inventor Charles H. Dennison personally, having worked with him in the context of preparing and prosecuting patent applications with which he was involved as an

inventor while he was in the employ of the Assignee of the present application, Micron Technology, Inc. in my capacity as outside counsel to Assignee. Mr. Dennison left the employ of Micron Technology, Inc. a number of years ago and is now in the employ of Ovonyx, Inc., a competitor of some product lines under development by the Assignee.

On April 1, 2005, I sent Mr. Dennison an email, a true copy of which is attached hereto as Exhibit A, requesting that he execute a Supplemental Reissue Declaration (Exhibit B). I also forwarded him a copy of original U.S. Patent 5,270,241 (Exhibit C), parent reissue U.S. Patent RE 38,049 (Exhibit D) and the pending claims of the present application (Exhibit E) for his reference.

Having received no response from Mr. Dennison, on May 2, 2005 I re-forwarded my email and attachments of April 1, 2005 (copy of email of May 2, 2005 without attachments appended hereto as Exhibit F) and again requested his assistance in executing the Supplemental Reissue Declaration.

On May 16, 2005 I called Mr. Dennison at his place of business, reached him at his desk, and asked 1) had he received my emails of April 1, 2005 and May 2, 2005 with the attachments, and 2) was he going to execute the proffered Supplemental Reissue Declaration. Mr. Dennison acknowledged receipt of the email and attachments, politely but unequivocally refused to execute the Supplemental Reissue Declaration, and the conversation was terminated.

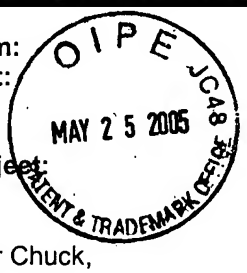
I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

May 26, 2005
Date

Joseph A. Walkowski

Document in ProLaw

Joseph Walkowski



From: Joseph Walkowski
Sent: Friday, April 01, 2005 3:36 PM
To: 'cdennison@ovonyx.com'
Cc: Debra Mitchell
Subject: Micron Reissue Application

Dear Chuck,

We have straightened out the claim language errors I noted in my email of Novmber 14, 2004 with regard to the pending reissue application, and I am sending you the following for your consideration in deciding whether you are in a position to execute the enclosed Supplemental Reissue Declaration:

1) PDF copy of US Patent 5270241
2) PDF copy of Reissue US Patent 38049
3) Microsoft Word copy of the allowed claims in the pending reissue application Serial No. 10/020,741, which is a continuation of #2. The specification and drawings are the same as in #1 and #2 above, so I am not sending these.

The Supplemental Reissue Declaration is also in Word.

If you would sign the Supplemental Reissue Declaration and fax it back to me at 801-531-9168 or scan it and send it as an email attachment, it would be most appreciated. If you have questions, I will be back in the office on April 7th, and please feel free to call me at 1-800-900-2001 or email me and I will respond upon my return.

Thank you very much for entertaining this request. I sincerely apologize for the imposition. We are just trying to do our job here at the firm.

Please give my best to Lia.

Joe Walkowski


US05270241.pdf (807 KB)


JSRE38049E.pdf (1 MB)


pending claims.doc (33 KB)


Suppl. Reissue Decl.doc (87 KB...

Exhibit A

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Dennison et al.

Serial No.: 10/020,741

Filed: December 12, 2001

For: OPTIMIZED CONTAINER STACKED CAPACITOR DRAM CELL UTILIZING SACRIFICIAL OXIDE DEPOSITION AND CHEMICAL MECHANICAL POLISHING

Confirmation No.: 2283

Examiner: T. Nguyen

Group Art Unit: 2813

Attorney Docket No.: 2269-3259.1US
(91-0473.02 RE)

CERTIFICATE OF MAILING

I hereby certify that this correspondence along with any attachments referred to or identified as being attached or enclosed is being deposited with the United States Postal Service as First Class Mail on the date of deposit shown below with sufficient postage and in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date _____ Signature _____

Doreen Neumann
Name (Type/Print)

SUPPLEMENTAL REISSUE DECLARATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

We hereby declare that:

Every error in the patent which was corrected in the present reissue application up to the time(s) of execution of this declaration by each of us, and which is not covered by the prior oath(s) and/or declaration(s) submitted in this application, arose without any deceptive intention on the part of the applicants.

We hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these

statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: _____

_____
Charles H. Dennison

Inventor's Full Name: Charles H. Dennison
Country of Citizenship: United States of America
Residence Address: 5719 Algonquin Way
San Jose, California 95138

Post Office Address: same as above

Date: _____

_____
Michael A. Walker

Inventor's Full Name: Michael A. Walker
Country of Citizenship: United States of America
Residence Address: 10866 Goldenrod
Boise, Idaho 83712

Post Office Address: same as above

Document in ProLaw

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Dennison et al.

Serial No.: 10/020,741

Filed: December 12, 2001

For: OPTIMIZED CONTAINER STACKED CAPACITOR DRAM CELL UTILIZING SACRIFICIAL OXIDE DEPOSITION AND CHEMICAL MECHANICAL POLISHING

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Group Art Unit: 2813

Attorney Docket No.: 2269-3259.1US
(91-0473.02 RE)

NOTICE OF EXPRESS MAILING

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Date of Deposit with USPS: May 26, 2005

Person making Deposit: Steve Wong

SUPPLEMENTAL REISSUE DECLARATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

We hereby declare that:

Every error in the patent which was corrected in the present reissue application up to the time(s) of execution of this declaration by each of us, and which is not covered by the prior oath(s) and/or declaration(s) submitted in this application, arose without any deceptive intention on the part of the applicants.

We hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these

statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: _____

_____
Charles H. Dennison

Inventor=s Full Name:	Charles H. Dennison
Country of Citizenship:	United States of America
Residence Address:	5719 Algonquin Way San Jose, California 95138
Post Office Address:	same as above

Date: April 6, 2005

_____
Michael A. Walker

Inventor=s Full Name:	Michael A. Walker
Country of Citizenship:	United States of America
Residence Address:	10866 Goldenrod Boise, Idaho 83712
Post Office Address:	same as above

Document in ProLaw

US005270241A

United States Patent [19]

Dennison et al.

[11] Patent Number: 5,270,241

[45] Date of Patent: * Dec. 14, 1993

[54] OPTIMIZED CONTAINER STACKED CAPACITOR DRAM CELL UTILIZING SACRIFICIAL OXIDE DEPOSITION AND CHEMICAL MECHANICAL POLISHING

[75] Inventors: Charles H. Dennison; Michael A. Walker, both of Boise, Id.

[73] Assignee: Micron Technology, Inc., Boise, Id.

[*] Notice: The portion of the term of this patent subsequent to Nov. 10, 2009 has been disclaimed.

[21] Appl. No.: 973,092

[22] Filed: Nov. 6, 1992

Related U.S. Application Data

[63] Continuation of Ser. No. 850,746, Mar. 13, 1992, Pat. No. 5,162,248.

[51] Int. Cl.[5] H01L 21/70

[52] U.S. Cl. 437/52; 437/47; 437/48; 437/60; 437/225; 437/919

[58] Field of Search 437/47, 48, 52, 60, 437/225, 228, 235, 919, 986; 257/306

[56] References Cited

U.S. PATENT DOCUMENTS

4,671,851	6/1987	Beyer et al.	156/648
4,944,836	7/1990	Beyer et al.	156/656
5,045,899	9/1991	Arimoto et al.	357/23.6

FOREIGN PATENT DOCUMENTS

0286270	12/1987	Japan	357/23.6
0074752	3/1989	Japan	357/919
0094554	4/1990	Japan	437/52

OTHER PUBLICATIONS

"Stacked Capacitor DRAM Cell with Vertical Fins" IBM TDB, Jul. 1990, pp. 245-247.

"Crown-Shaped Stacked-Capacitor Cell for 1.5-V Operation 64-Mb Dram's" by T. Kaga et al., IEEE Transactions on Electron Devices, vol. 38, No. 2, Feb. 1991, pp. 255-261.

"A Stacked Capacitor Cell with Ring Structure" by N. Shinmura et al., pp. 833-836. (Extended abstracts of the 22rd International Conference on Solid State Devices, 1990).

Primary Examiner—Tom Thomas

Attorney, Agent, or Firm—David J. Paul

[57] ABSTRACT

An existing stacked capacitor fabrication process is modified to construct a three-dimensional stacked container capacitor. The present invention develops the container capacitor by etching an opening (or contact opening) into a low etch rate oxide. The contact opening is used as a form for deposited polysilicon that conforms to the sides of the opening walls. Within the thin poly lining of the oxide container a high etch-rate oxide, such as ozone TEOS, is deposited over the entire structure thereby bridging across the top of the oxide container. The high etch-rate oxide is planarized back to the thin poly and the resulting exposed poly is then removed to separate neighboring containers. The two oxides, having different etch rates, are then etched thereby leaving a free-standing poly container cell with 100% (or all) of the higher etch rate oxide removed and a pre-determined oxide surrounding the container still intact.

60 Claims, 4 Drawing Sheets

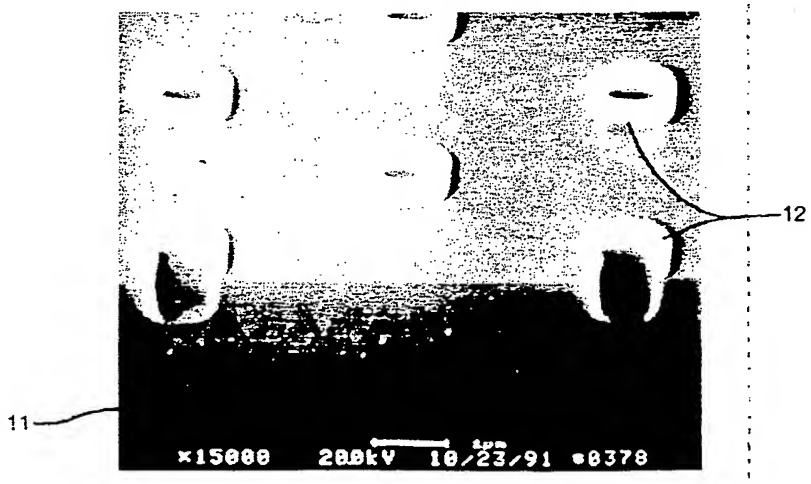

Exhibit C

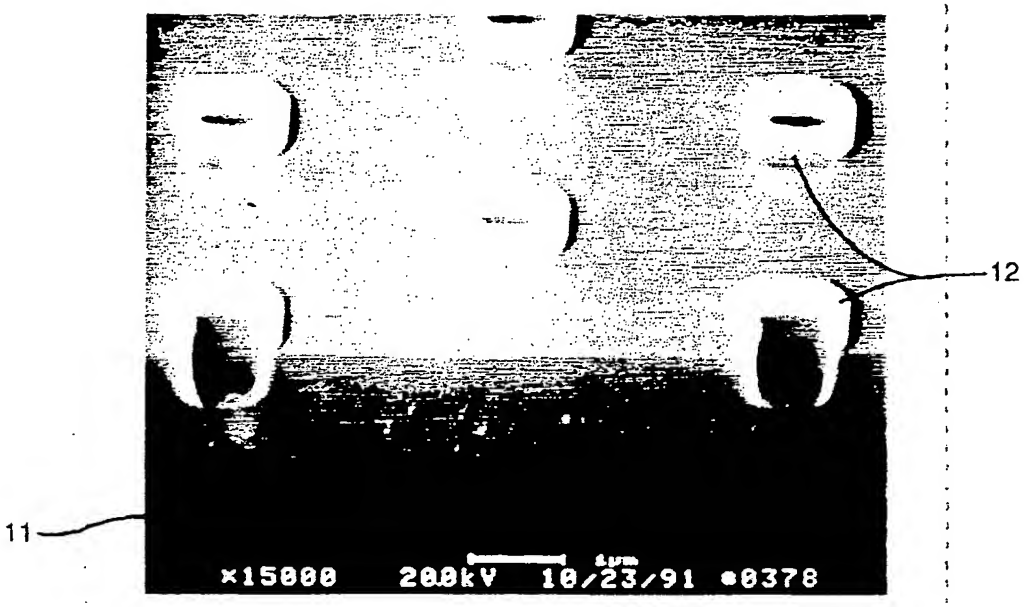

FIG. 1

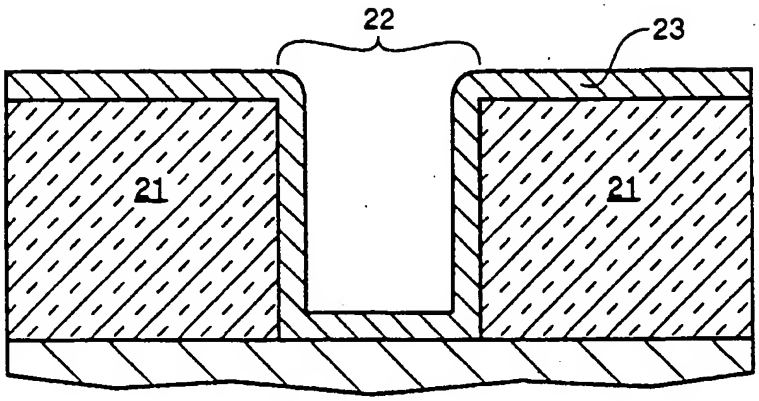

FIG. 2

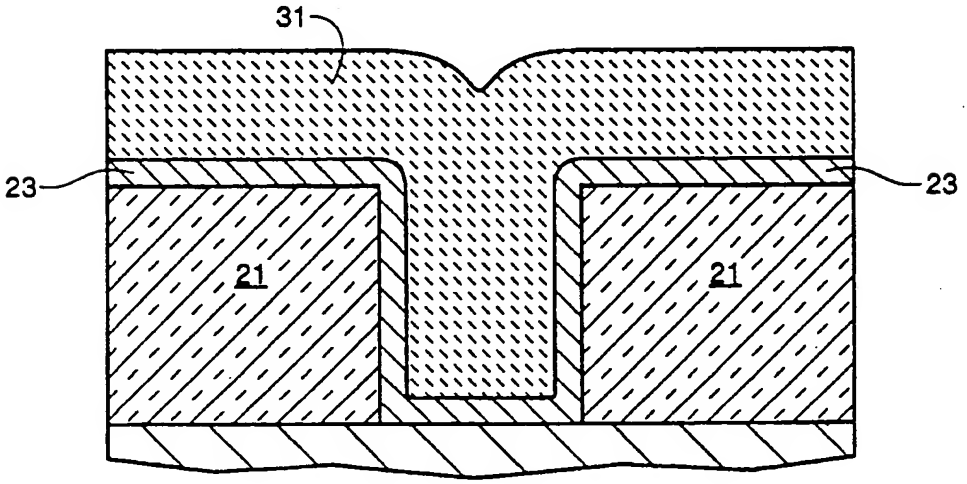

FIG. 3

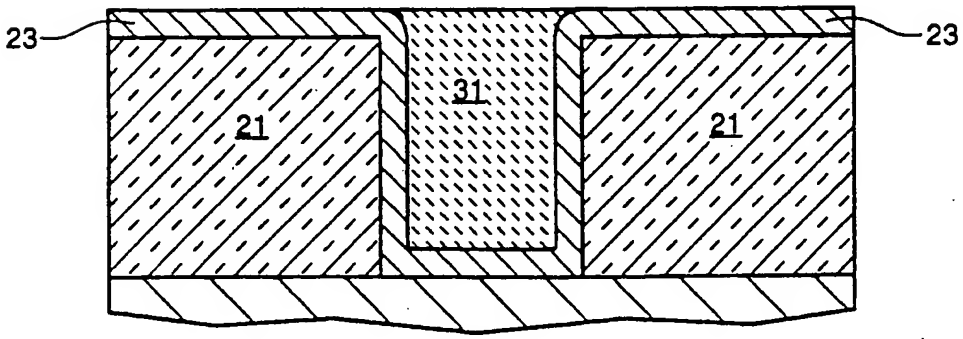

FIG. 4

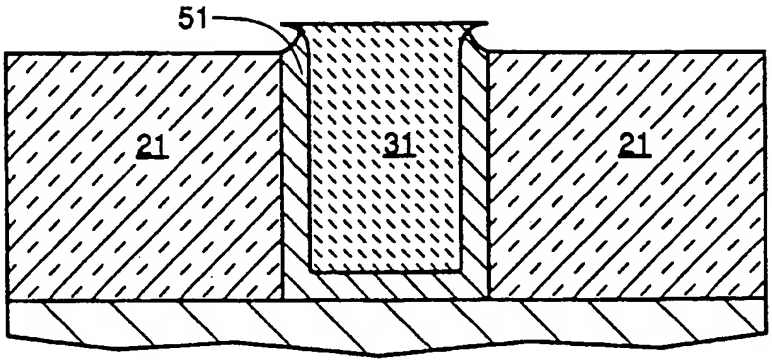

FIG. 5

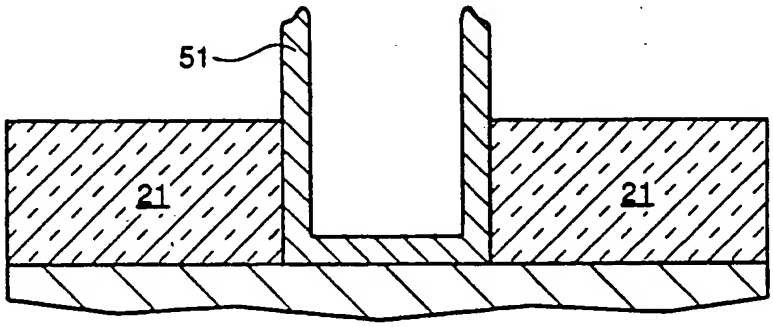

FIG. 6

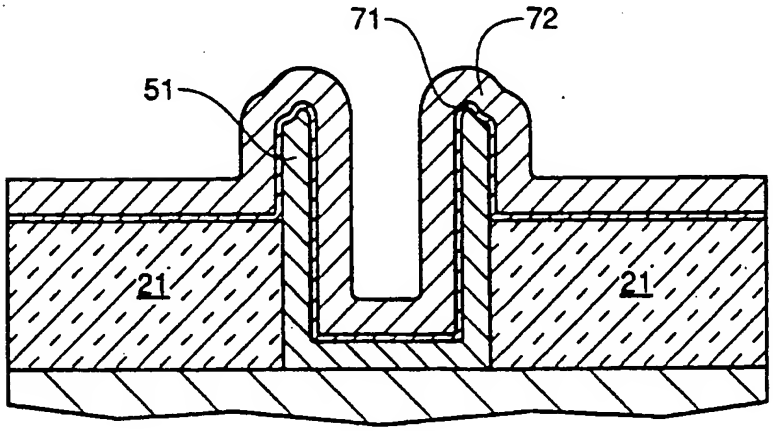

FIG. 7

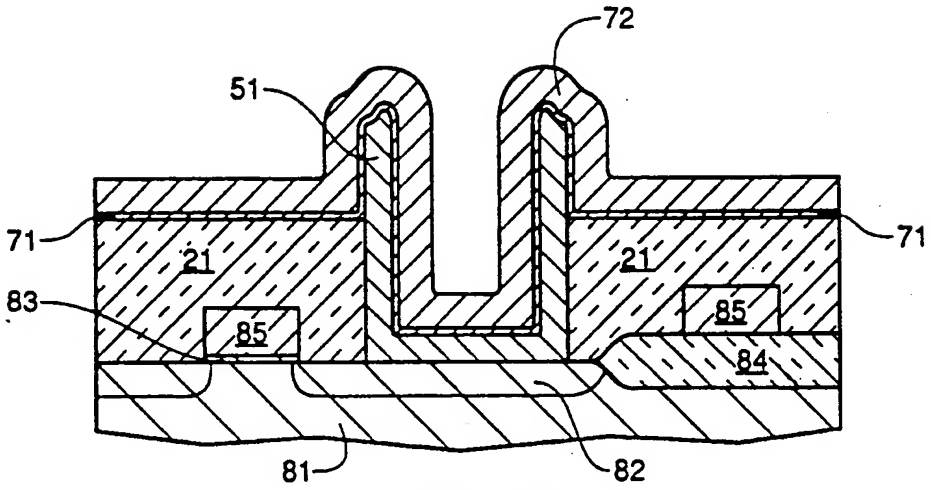

FIG. 8

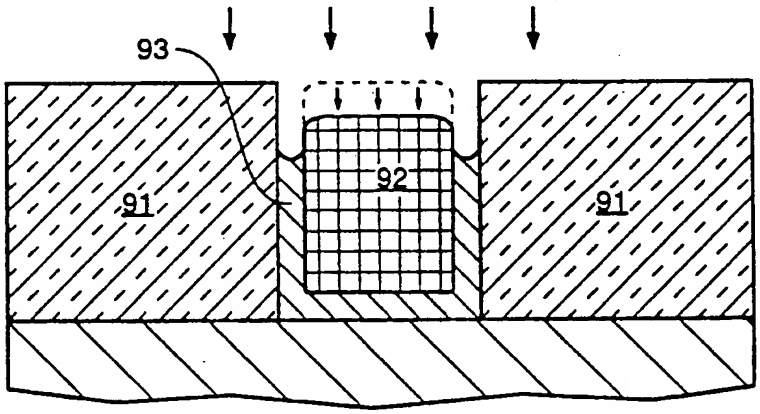

FIG. 9

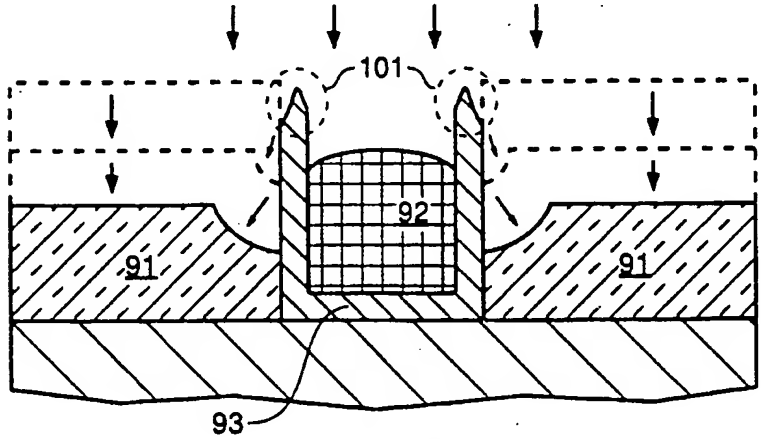

FIG. 10

OPTIMIZED CONTAINER STACKED CAPACITOR DRAM CELL UTILIZING SACRIFICIAL OXIDE DEPOSITION AND CHEMICAL MECHANICAL POLISHING

CROSS-REFERENCE TO RELATED APPLICATION

This is a continuation to U.S. patent application Ser. No. 07/850,746, filed Mar. 13, 1992, now U.S. Pat. No. 5,162,248.

FIELD OF THE INVENTION

This invention relates to semiconductor circuit memory storage devices and more particularly to a process for fabricating three-dimensional stacked capacitor structures that may be used in such storage devices as high-density dynamic random access memories (DRAMs).

BACKGROUND OF THE INVENTION

In dynamic semiconductor memory storage devices it is essential that storage node capacitor cell plates be large enough to retain an adequate charge or capacitance in spite of parasitic capacitances and noise that may be present during circuit operation. As is the case for most semiconductor integrated circuitry, circuit density is continuing to increase at a fairly constant rate. The issue of maintaining storage node capacitance is particularly important as the density of DRAM arrays continues to increase for future generations of memory devices.

The ability to densely pack storage cells while maintaining required capacitance levels is a crucial requirement of semiconductor manufacturing technologies if future generations of expanded memory array devices are to be successfully manufactured.

One method of maintaining, as well as increasing, storage node size in densely packed memory devices is through the use of "stacked storage cell" design. With this technology, two or more layers of a conductive material such as polycrystalline silicon (polysilicon or poly) are deposited over an access device on a silicon wafer, with dielectric layers sandwiched between each poly layer. A cell constructed in this manner is known as a stacked capacitor cell (STC). Such a cell utilizes the space over the access device for capacitor plates, has a low soft error rate (SER) and may be used in conjunction with inter-plate insulative layers having a high dielectric constant.

However, it is difficult to obtain sufficient storage capacitance with a conventional STC capacitor as the storage electrode area is confined within the limits of its own cell area. Also, maintaining good dielectric breakdown characteristics between poly layers in the STC capacitor becomes a major concern once insulator thickness is appropriately scaled.

A paper submitted by N. Shinmura, et al., entitled "A Stacked Capacitor Cell with Ring Structure," Extended Abstracts of the 22nd International Conference on Solid State Devices and Materials, 1990, pp. 833-836, discusses a 3-dimensional stacked capacitor incorporating a ring structure around the main electrode to effectively double the capacitance of a conventional stacked capacitor.

The ring structure and its development is shown in FIGS. 1(*c*) through 1(*g*), pp. 834 of the article mentioned above. FIG. 1(*a*), on the same page shows a bird's eye-view of storage electrodes. The storage node is formed by two polysilicon layers that form a core electrode encircled by a ring structure. Capacitor dielectric film surrounds the whole surface of the storage node electrode and then is covered with a third polysilicon layer to form the top capacitor electrode and completes the storage cell. This design can be fabricated using current methods and increases storage capacitance by as much as 200%.

Also, in a paper submitted by T. Kaga, et al., entitled "Crown-Shaped Stacked-Capacitor Cell for 1.5-V Operation 64-Mb DRAM's," IEEE Transactions on Electron Devices. VOL. 38, NO. 2, February 1991, pp. 255-261, discusses a self-aligned stacked-capacitor cell for 64-Mb DRAM's, called a CROWN cell. The CROWN cell and its development are shown in FIGS. 7(*d*) through 7(*f*), pp. 258 of this article. The crown shaped storage electrode is formed over word and bit lines and separated by a oxide/nitride insulating layer with the top insulating layer being removed to form the crown shape. Capacitor dielectric film surrounds the whole surface of the storage node electrode and the top capacitor electrode is formed to complete the storage cell.

The present invention develops an existing stacked capacitor fabrication process to construct and optimize a three-dimensional container stacked capacitor cell. The capacitor's bottom plate (or storage node plate) is centered over a buried contact (or node contact) connected to an access transistor's diffusion area. The method presented herein provides fabrication uniformity and repeatability of the three-dimensional container cell.

SUMMARY OF THE INVENTION

The invention is directed to maximizing storage cell surface area in a high density/high volume DRAM (dynamic random access memory) fabrication process. An existing capacitor fabrication process is modified to construct a three-dimensional stacked container capacitor. The capacitor design of the present invention defines a stacked capacitor storage cell that is used in a DRAM process, however it will be evident to one skilled in the art to incorporate these steps into other processes requiring volatile memory cells, such as VRAMs or the like.

After a silicon wafer is prepared using conventional process steps, the present invention develops the container capacitor by etching a contact opening into a low etch rate oxide. The contact opening is used as a form for deposited polysilicon that conforms to the sides of the opening walls. Within the thin poly lining of the oxide container a high etch-rate oxide, such as ozone TEOS, is deposited over the entire structure thereby bridging across the top of the oxide container. The high etch-rate oxide is planarized back to the thin poly by using Chemical Mechanical Polishing (CMP). This CMP step is selective such that oxide is removed with sufficient overetch and stops on the thin poly. The resulting exposed poly is then removed to separate neighboring containers either through an isotropic wet poly etch or an additional CMP with the chemical aspect modified to now etch and selectively remove the poly and not the oxide. The two oxides, having different etch rates, are then etched by a single wet dilute BOE etch step, thereby leaving a free-standing poly container cell, with all the inside (high etch rate) oxide removed, that

is equal in height to the depth of the original contact opening. In addition, a pre-determined amount of low etch rate oxide is removed thereby leaving oxide surrounding the ,container, poly for both structural support and process integration for further processing which requires oxide to be left above the word lines.

The present invention uses a higher etch-rate oxide inside the container to block the container poly etch. This high etch rate oxide is completely removed during oxide etch back. This protects the container during processing without adding photoresist and introducing extra processing steps or unwarranted contaminants. A standard CMP oxide etch is utilized that allows fabrication uniformity and repeatability across the wafer which cannot be achieved by resist filled container processes.

Another advantage of filling the container with high etch rate oxide is that the poly can be etched with a low cost, timed wet poly etch, while partially filled containers (as seen in FIG. 9), due to inherent recession of resist 92 height (to allow for sufficient process margin), will not allow a wet poly etch without loss in cell height 93, loss in uniformity and repeatability across the wafer's surface. Because this invention can be etched isotropically at poly etch, it avoids the recessing (overetch of the storage poly container 93 in FIG. 9) and splintering effects caused by a dry etch poly process.

As seen in FIG. 10, splintering effects 101 of storage node poly 93 result from a dry anisotropic etch (due to non-uniform etching of polycrystalline silicon 93) because the plasma etch reacts faster along heavily doped grain boundaries. Splinters 101 later tend to 'break off' in subsequent processing leading to contamination particulates. The trenching of the poly leads to the sidewalls of the poly container to be exposed, thus making it impossible to wet etch the oxide around the cell without translating the trenched poly horizontal portion of the etch into surrounding oxide 91 thereby leaving a ring of thin oxide around he container cell.

The present invention also protects the vertical sidewall of the oxide form by covering it with poly, thereby making a horizontal wet oxide etch back possible. In addition, all films which see etch processing, CMP or otherwise, are subsequently removed thereby acting as sacrificial films such that particles created during the CMP etch do not contaminate the inside of the poly container.

FIG. 1 shows a gray scale reproduction of a SEM photograph of an array of poly containers 12 which demonstrates the uniformity and repeatability of poly containers 12 across substrate that results from utilizing the process steps of the present invention discussed hereinafter.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a gray-scale reproduction of a SEM (Scanning Electronic Microscope) photograph of a cross-sectional view of an array of container poly rings;

FIG. 2 is a composite cross-sectional view of an in-process wafer portion depicting the beginning steps of the present invention, said steps comprising forming a planarized layer of low etch rate oxide, etching a buried contact and placing a thin layer of conformal poly;

FIG. 3 is a cross-sectional view of the in-process wafer portion of FIG. 2 after formation of a layer of high etch rate oxide;

FIG. 4 is a cross-sectional view of the in-process wafer portion of FIG. 3 after planarization of the high etch rate oxide;

FIG. 5 is a cross-sectional view of the in-process wafer portion of FIG. 4 following a wet etch back of the exposed thin poly layer;

FIG. 6 is a cross-sectional view of the in-process wafer portion of FIG. 5 following an etch of both low etch rate and high etch rate oxides;

FIG. 7 is a cross-sectional view of the in-process wafer portion FIG. 6 following blanket formations of conformal cell dielectric and polysilicon, respectively;

FIG. 8 is a cross-sectional view of a storage cell created by the present invention when integrated into a stacked capacitor fabrication process; and

FIG. 9 is a composite cross-sectional view of an in-process wafer portion depicting a container cell filled with photoresist prior to patterning; and

FIG. 10 is a composite cross-sectional view of the in-process wafer portion of FIG. 9 depicting splintering of storage node poly and formation of a thin ring of oxide surrounding the storage node poly following an anisotropic etching to pattern a container cell.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The invention is directed to maximizing storage cell surface area, as well as providing uniform and repeatable, defect free, storage cell structures across a given substrate, in a high density/high volume DRAM fabrication process, in a sequence shown in FIGS. 2-7.

A silicon wafer is prepared using conventional process steps up to the point of processing an array of storage cell capacitors. Capacitor cell fabrication will now follow.

The storage capacitor of each memory cell will make contact directly to an underlying diffusion area. Each underlying diffusion area will have two storage node connections isolated from a single digit line contact by access transistors formed by poly word lines crossing the active area. Normally each diffusion area within the array is isolated from one another by a thick field oxide. The diffusion areas can be arranged in interdigitated columns and non-interdigitated rows or simply parallel and in line to one another in both the vertical and horizontal directions. As previously mentioned, the diffusion areas are used to form active MOS transistors (serving as access transistors to each individual capacitor) that can be doped as NMOS or PMOS type FETs depending on the desired use.

Referring now to FIG. 2, a thick layer of low etch rate oxide 21 is formed over an existing topography of a given substrate. Oxide 21 is then planarized, preferably by chemical-mechanical planarization (CMP) techniques down to a predetermined thickness. The thickness of planarized oxide 21 depends on the height that is desired for the poly container structure yet to be formed. The height of the resulting poly structure will determine the capacitor plate surface area that will be required to sufficiently hold a charge. It has been shown that a structure of approximately 1.0–1.5μ is sufficient to construct a reliable 64M DRAM cell using optimized cell dielectric (Container height depends on such factors as container diameter, dielectric constant and thickness of oxides used which are brought to light in the continuing discussion.). A contact opening 22 is then etched into oxide 21 thereby allowing access to the underlying topography (for DRAM capacitor purposes

this opening would normally expose a diffusion region conductively doped into a starting substrate). Contact opening **22** not only allows access to the underlying topography but also provides a form for a subsequent placed layer of thin poly. This thin poly is now formed, preferably by CVD, as a layer of conformal polysilicon **23** and is placed overlying planarized oxide **21**, the patterned edges of oxide **21** and the exposed underlying topography. Poly **23** may either have been deposited insitu doped or deposited insitu doped and rugged HSG poly for added cell capacitance or it may be subsequently doped.

Referring now to FIG. **3**, a thick layer of oxide **31** having a high etch rate is formed over poly **23**. Oxide **31** is thick enough to completely fill the poly lined contact opening **22**.

Referring now to FIG. **4**, oxide layer **31** is removed down to poly **23**, preferably by CMP which will selectively stop on the first exposed upper regions of poly **23**.

Referring now to FIG. **5**, the exposed upper portions of poly **23** are removed to separate neighboring poly structures thereby forming individual containers **51** residing in contact openings **22** and exposing underlying oxide **21**. The areas of poly **23** that are removed may be accomplished by performing a poly etch selective to oxide, which could be a timed wet etch or an optimized CMP poly etch. A very significant advantage of this process flow when a CMP etch step is utilized is that the inside of the future container **51** is protected from 'slurry' contamination that is inherent in the CMP step which proves difficult to remove in high aspect ratio storage containers (0.5μ inside diameter by 1.5μ high).

Referring now to FIG. **6**, both oxides **21** and **31**, which have different etch rates, are now exposed. At this point, an oxide etch is performed such that oxide **31** is completely removed from inside container **51** while a portion of oxide **21** remains at the base of container **51** and thereby providing an insulating layer between the underlying topography and subsequent layers. A etch rate ratio of 2:1 or greater between (a ratio of 4:1 is preferred) oxide **31** and oxide **22** provides sufficient process margin to ensure all of high etch rate oxide **31** inside container **51** is removed during the single etch step, while a portion of oxide **22** remains to provide adequate insulation from subsequently formed layers.

Referring now to FIG. **7**, when using this structure to form a capacitor storage node plate container **51** and the remaining portion of oxide **21** is coated with a capacitor cell dielectric **71**. And, finally a second conformal poly layer **72** is placed to blanket cell dielectric **71** and serves as a common capacitor cell plate to the entire array of containers **51**. From this point on the wafer is completed using conventional fabrication process steps.

FIG. **8** depicts a cross-section of the present invention integrated into a stacked capacitor process on starting substrate **81**. Container **51** connects to diffusion area **82** and thereby serves as a storage node container plate. Diffusion area **82** is accessed by word line **85** (separated by gate insulator **83**) which in turn spans the channel's active area between diffusion areas **82**. The poly of container **51** is doped to the same conductivity type as underlying diffusion region **82** to insure a good ohmic contact.

It is to be understood that although the present invention has been described with reference to a preferred embodiment, various modifications, known to those skilled in the art, may be made to the structures and process steps presented herein without departing from the invention as recited in the several claims appended hereto.

We claim:

1. A process for fabricating a uniform and repeatable conductive container structure on a starting substrate's existing topography, said process comprising the steps of:

a) forming a blanketing first insulating layer, having a first etch rate, over said existing topography;

b) patterning and etching an opening into said first insulating layer, said opening thereby forming a container form;

c) forming a conformal first conductive layer superjacent said first insulating layer and said container form thereby lining said container form;

d) forming a blanketing second insulating layer, having a second etch rate, superjacent said first conductive layer;

e) removing said second insulating layer via chemical mechanical planarization until upper portion of said first conductive layer is exposed;

f) removing said exposed first conductive upper layer until underlying said first insulating layer is exposed thereby separating said first conductive layer into individual said conductive containers having inner and outer walls;

g) removing said first and said second insulating layers such that said second insulating layer is completely removed thereby exposing the entire inner walls of said conductive container and said first insulating layer is partially removed thereby exposing an upper portion of said outer walls of said conductive container, wherein the partially remaining first insulating layer provides insulation between said underlying substrate topography and subsequently formed layers;

h) forming a third insulating layer superjacent and coextensive said exposed walls and inner bottom portion of said container and said partially remaining first insulating layer; and

i) forming a second conductive layer superjacent and coextensive said third insulating layer.

2. A process as recited in claim **1**, wherein said first insulating layer is planarized prior to said step of patterning and etching an opening into said first insulating layer.

3. A process as recited in claim **1**, wherein said second insulating layer is a sacrificial layer conducive to said chemical mechanical planarization.

4. A process as recited in claim **1**, wherein said first and said second insulating layers are oxides.

5. A process as recited in claim **1**, wherein said first insulating layer etch rate is a lower etch rate than said second insulating layer etch rate.

6. A process as recited in claim **5**, wherein the etch rate ratio between said second insulating layer etch rate and said first insulating layer etch rate is a ratio of 2:1 or greater.

7. A process as recited in claim **5**, wherein the etch rate ratio between said second insulating layer etch rate and said first insulating layer etch rate is a ratio of 4:1.

8. A process as recited in claim **1**, wherein said first and said second conductive layers are doped polysilicon.

9. A process as recited in claim **8**, wherein said doped polysilicon is formed by insitu doped chemical vapor deposition.

10. A process as recited in claim 1, wherein said first, said second and said third insulating layers are formed by chemical vapor deposition.

11. A process for fabricating a uniform and repeatable conductive container structure on a starting substrate's existing topography, said process comprising the steps of:

a) forming a blanketing first insulating layer, having a first etch rate, over said existing topography;

b) patterning and etching an opening into said first insulating layer, said opening thereby forming a container form;

c) forming a conformal first conductive layer superjacent said first insulating layer and said container form thereby lining said container form;

d) forming a blanketing second insulating layer, having a second etch rate, superjacent said first conductive layer;

e) removing said second insulating layer until upper portion of said first conductive layer is exposed;

f) removing said exposed first conductive upper layer via chemical mechanical planarization until underlying said first insulating layer is exposed thereby separating said first conductive layer into individual said conductive containers having inner and outer walls;

g) removing said first and said second insulating layers such that said second insulating layer is completely removed thereby exposing the entire inner walls of said conductive container and said first insulating layer is partially removed thereby exposing an upper portion of said outer walls of said conductive container, wherein the partially remaining first insulating layer provides insulation between said underlying substrate topography and subsequently formed layers;

h) forming a third insulating layer superjacent and coextensive said exposed walls and inner bottom portion of said container and said partially remaining first insulating layer; and

i) forming a second conductive layer superjacent and coextensive said third insulating layer.

12. A process as recited in claim 1, wherein said first insulating layer is planarized prior to said step of patterning and etching an opening into said first insulating layer.

13. A process as recited in claim 1, wherein said second insulating layer is a sacrificial layer that is planarized by chemical mechanical planarization.

14. A process as recited in claim 1, wherein said first and said second insulating layers are oxides.

15. A process as recited in claim 1, wherein said first insulating layer etch rate is a lower etch rate than said second insulating layer etch rate.

16. A process as recited in claim 15, wherein the etch rate ratio between said second insulating layer etch rate and said first insulating layer etch rate is a ratio of 2:1 or greater.

17. A process as recited in claim 15, wherein the etch rate ratio between said second insulating layer etch rate and said first insulating layer etch rate is a ratio of 4:1.

18. A process as recited in claim 1, wherein said first and said second conductive layers are doped polysilicon.

19. A process as recited in claim 18, wherein said doped polysilicon is formed by insitu doped chemical vapor deposition.

20. A process as recited in claim 1, wherein said first, said second and said third insulating layers are formed by chemical vapor deposition.

21. A process for fabricating a uniform and repeatable conductive container structure on a starting substrate's existing topography, said process comprising the steps of:

a) forming a blanketing first insulating layer, having a first etch rate, over said existing topography;

b) patterning and etching an opening into said first insulating layer, said opening thereby forming a container form;

c) forming a conformal first conductive layer superjacent said first insulating layer and said container form thereby lining said container form;

d) forming a blanketing second insulating layer, having a second etch rate, superjacent said first conductive layer;

e) removing said second insulating layer via chemical mechanical planarization until upper portion of said first conductive layer is exposed;

f) removing said exposed first conductive upper layer via chemical mechanical planarization until underlying said first insulating layer is exposed thereby separating said first conductive layer into individual said conductive containers having inner and outer walls;

g) removing said first and said second insulating layers such that said second insulating layer is completely removed thereby exposing the entire inner walls of said conductive container and said first insulating layer is partially removed thereby exposing an upper portion of said outer walls of said conductive container, wherein the partially remaining first insulating layer provides insulation between said underlying substrate topography and subsequently formed layers;

h) forming a third insulating layer superjacent and coextensive said exposed walls and inner bottom portion of said container and said partially remaining first insulating layer; and

i) forming a second conductive layer superjacent and coextensive said third insulating layer.

22. A process as recited in claim 21, wherein said first insulating layer is planarized prior to said step of patterning and etching an opening into said first insulating layer.

23. A process as recited in claim 21, wherein said second insulating layer is a sacrificial layer conducive to said chemical mechanical planarization.

24. A process as recited in claim 21, wherein said first and said second insulating layers are oxides.

25. A process as recited in claim 21, wherein said first insulating layer etch rate is a lower etch rate than said second insulating layer etch rate.

26. A process as recited in claim 25, wherein the etch rate ratio between said second insulating layer etch rate and said first insulating layer etch rate is a ratio of 2:1 or greater.

27. A process as recited in claim 25, wherein the etch rate ratio between said second insulating layer etch rate and said first insulating layer etch rate is a ratio ob 4:1.

28. A process as recited in claim 21, wherein said first and said second conductive layers are doped polysilicon.

29. A process as recited in claim 28, wherein said doped polysilicon is formed by insitu doped chemical vapor deposition.

30. A process as recited in claim 21, wherein said first, said second and said third insulating layers are formed by chemical vapor deposition.

31. A process for fabricating a DRAM container storage capacitor on a silicon substrate having active areas, word lines and digit lines, said process comprising the following sequence of steps:

a) forming a blanketing first insulating layer, having a first etch rate, over said existing topography;

b) patterning and etching an opening into said first insulating layer, said opening thereby forming a container form;

c) forming a conformal first conductive layer superjacent said first insulating layer and said container form thereby lining said container form;

d) forming a blanketing second insulating layer, having a second etch rate, superjacent said first conductive layer;

e) removing said second insulating layer via chemical mechanical planarization until upper portion of said first conductive layer is exposed;

f) removing said exposed first conductive upper layer until underlying said first insulating layer is exposed thereby separating said first conductive layer into individual said container storage capacitors having inner and outer walls;

g) removing said first and said second insulating layers such that said second insulating layer is completely removed thereby exposing the entire inner walls of said container storage capacitor and said first insulating layer is partially removed thereby exposing an upper portion of said outer walls of said container storage capacitor, wherein the partially remaining first insulating layer provides insulation between said underlying substrate topography and subsequently formed layers;

h) forming a third insulating layer superjacent and coextensive said exposed walls and inner bottom portion of said capacitor and said partially remaining first insulating layer; and

i) forming a second conductive layer superjacent and coextensive said third insulating layer.

32. A process as recited in claim 31, wherein said first insulating layer is planarized prior to said step of patterning and etching an opening into said first insulating layer.

33. A process as recited in claim 31, wherein said second insulating layer is a sacrificial layer conductive to said chemical mechanical planarization.

34. A process as recited in claim 31, wherein said first and said second insulating layers are oxides.

35. A process as recited in claim 31, wherein said first insulating layer etch rate is a lower etch rate than said second insulating layer etch rate.

36. A process as recited in claim 35, wherein the etch rate ratio between said second insulating layer etch rate and said first insulating layer etch rate is a ratio of 2:1 or greater.

37. A process as recited in claim 35, wherein the etch rate ratio between said second insulating layer etch rate and said first insulating layer etch rate is a ratio of 4:1.

38. A process as recited in claim 31, wherein said first and said second conductive layers are doped polysilicon.

39. A process as recited in claim 38, wherein said doped polysilicon is formed by insitu doped chemical vapor deposition.

40. A process as recited in claim 31, wherein said first, said second and said third insulating layers are formed by chemical vapor deposition.

41. A process for fabricating a DRAM container storage capacitor on a silicon substrate having active areas, word lines and digit lines, said process comprising the following sequence of steps:

a) forming a blanketing first insulating layer, having a first etch rate, over said existing topography;

b) patterning and etching an opening into said first insulating layer, said opening thereby forming a container form;

c) forming a conformal first conductive layer superjacent said first insulating layer and said container form thereby lining said container form.

d) forming a blanketing second insulating layer, having a second etch rate, superjacent said first conductive layer;

e) removing said second insulating layer until upper portion of said first conductive layer is exposed;

f) removing said exposed first conductive upper layer via chemical mechanical planarization until underlying said first insulating layer is exposed thereby separating said first conductive layer into individual said container storage capacitors having inner and outer walls;

g) removing said first and said second insulating layers such that said second insulating layer is completely removed thereby exposing the entire inner walls of said container storage capacitor and said first insulating layer is partially removed thereby exposing an upper portion of said outer walls of said container storage capacitor, wherein the partially remaining first insulating layer provides insulation between said underlying substrate topography and subsequently formed layers;

h) forming a third insulating layer superjacent and coextensive said exposed walls and inner bottom portion of said capacitor and said partially remaining first insulating layer; and

i) forming a second conductive layer superjacent and coextensive said third insulating layer.

42. A process as recited in claim 41, wherein said first insulating layer is planarized prior to said step of patterning and etching an opening into said first insulating layer.

43. A process as recited in claim 41, wherein said second insulating layer is a sacrificial layer that is planarized by chemical mechanical planarization.

44. A process as recited in claim 41, wherein said first and said second insulating layers are oxides.

45. A process as recited in claim 41, wherein said first insulating layer etch rate is a lower etch rate than said second insulating layer etch rate.

46. A process as recited in claim 45, wherein the etch rate ratio between said second insulating layer etch rate and said first insulating layer etch rate is a ratio of 2:1 or greater.

47. A process as recited in claim 45, wherein the etch rate ratio between said second insulating layer etch rate and said first insulating layer etch rate is a ratio of 4:1.

48. A process as recited in claim 41, wherein said first and said second conductive layers are doped polysilicon.

49. A process as recited in claim 48, wherein said doped polysilicon is formed by insitu doped chemical vapor deposition.

50. A process as recited in claim **41**, wherein said first, said second and said third insulating layers are formed by chemical vapor deposition.

51. A process for fabricating a DRAM container storage capacitor on a silicon substrate having active areas, word lines and digit lines, said process comprising the following sequence of steps:

a) forming a blanketing first insulating layer, having a first etch rate, over said existing topography;

b) patterning and etching an opening into said first insulating layer, said opening thereby forming a container form;

c) forming a conformal first conductive layer superjacent said first insulating layer and said container form thereby lining said container form;

d) forming a blanketing second insulating layer, having a second etch rate, superjacent said first conductive layer;

e) removing said second insulating layer via chemical mechanical planarization until upper portion of said first conductive layer is exposed;

f) removing said exposed first conductive upper layer via chemical mechanical planarization until underlying said first insulating layer is exposed thereby separating said first conductive layer into individual said container storage capacitors having inner and outer walls;

g) removing said first and said second insulating layers such that said second insulating layer is completely removed thereby exposing the entire inner walls of said container storage capacitor and said first insulating layer is partially removed thereby exposing an upper portion of said outer walls of said container storage capacitor, wherein the partially remaining first insulating layer provides insulation between said underlying substrate topography and subsequently formed layers;

h) forming a third insulating layer superjacent and coextensive said exposed walls and inner bottom portion of said capacitor and said partially remaining first insulating layer; and

i) forming a second conductive layer superjacent and coextensive said third insulating layer.

52. A process as recited in claim **51**, wherein said first insulating layer is planarized prior to said step of patterning and etching an opening into said first insulating layer.

53. A process as recited in claim **51**, wherein said second insulating layer is a sacrificial layer conducive to said chemical mechanical planarization.

54. A process as recited in claim **51**, wherein said first and said second insulating layers are oxides.

55. A process as recited in claim **51**, wherein said first insulating layer etch rate is a lower etch rate than said second insulating layer etch rate.

56. A process as recited in claim **55**, wherein the etch rate ratio between said second insulating layer etch rate and said first insulating layer etch rate is a ratio of 2:1 or greater.

57. A process as recited in claim **55**, wherein the etch rate ratio between said second insulating layer etch rate and said first insulating layer etch rate is a ratio of 4:1.

58. A process as recited in claim **51**, wherein said first and said second conductive layers are doped polysilicon.

59. A process as recited in claim **58**, wherein said doped polysilicon is formed by insitu doped chemical vapor deposition.

60. A process as recited in claim **51**, wherein said first, said second and said third insulating layers are formed by chemical vapor deposition.

* * * * *

US00RE38049E

(19) **United States**

(12) **Reissued Patent**

Dennison et al.

(10) **Patent Number: US RE38,049 E**

(45) **Date of Reissued Patent: Mar. 25, 2003**

(54) **OPTIMIZED CONTAINER STACKED CAPACITOR DRAM CELL UTILIZING SACRIFICIAL OXIDE DEPOSITION AND CHEMICAL MECHANICAL POLISHING**

(75) Inventors: **Charles H. Dennison**, Meridian, ID (US); **Michael A. Walker**, Boise, ID (US)

(73) Assignee: **Micron Technology, Inc.**, Boise, ID (US)

(21) Appl. No.: **08/759,058**

(22) Filed: **Oct. 7, 1996**

Related U.S. Patent Documents

Reissue of:

(64) Patent No.: **5,270,241**
Issued: **Dec. 14, 1993**
Appl. No.: **07/973,092**
Filed: **Nov. 6, 1992**

U.S. Applications:

(63) Continuation of application No. 07/850,746, filed on Mar. 13, 1992, now Pat. No. 5,162,248.

(51) **Int. Cl.**[7] **H01L 21/20**

(52) **U.S. Cl.** **438/396**; 438/253; 438/238; 438/692; 438/633; 216/6

(58) **Field of Search** 148/DIG. 14; 438/396, 438/397, 398, 253, 254, 255, 238, 692, 633; 216/633, 6

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Primary Examiner—Tuan H. Nguyen

(74) *Attorney, Agent, or Firm*—Traskbritt

(57) **ABSTRACT**

An existing stacked capacitor fabrication process is modified to construct a three-dimensional stacked container capacitor. The present invention develops the container capacitor by etching an opening (or contact opening) into a low etch rate oxide. The contact opening is used as a form for deposited polysilicon that conforms to the sides of the opening walls. Within the thin poly lining of the oxide container a high etch-rate oxide, such as ozone TEOS, is deposited over the entire structure thereby bridging across the top of the oxide container. The high etch-rate oxide is planarized back to the thin poly and the resulting exposed poly is then removed to separate neighboring containers. The two oxides, having different etch rates, are then etched thereby leaving a free-standing poly container cell with 100% (or all) of the higher etch rate oxide removed and a pre-determined oxide surrounding the container still intact.

66 Claims, 4 Drawing Sheets

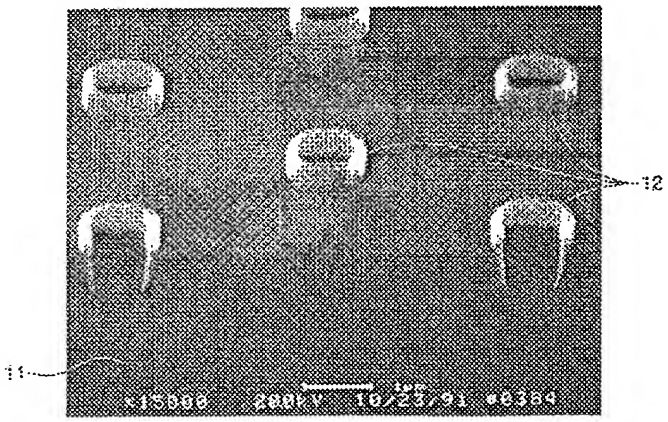


Exhibit D

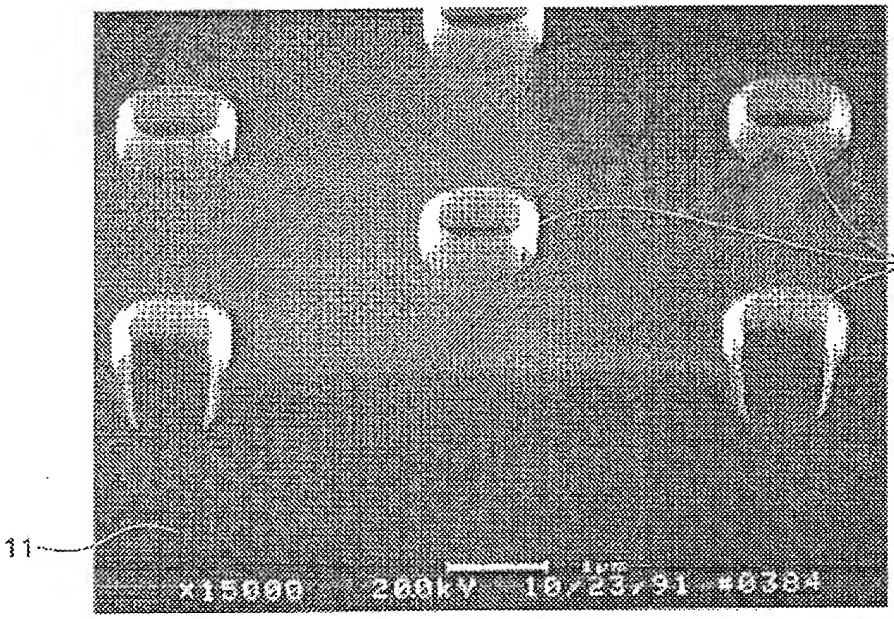


FIG. 1

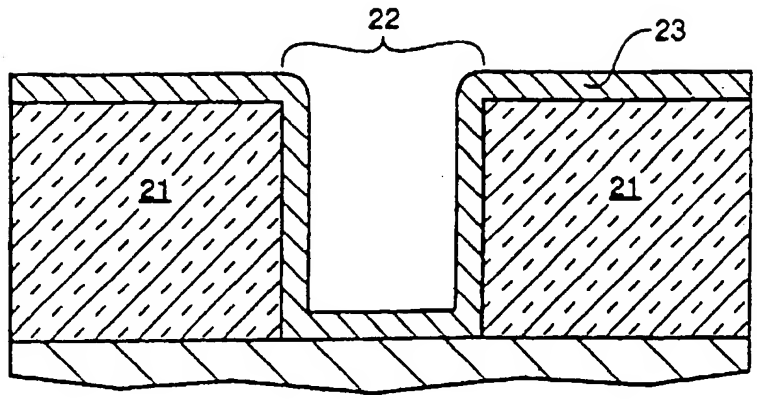


FIG. 2

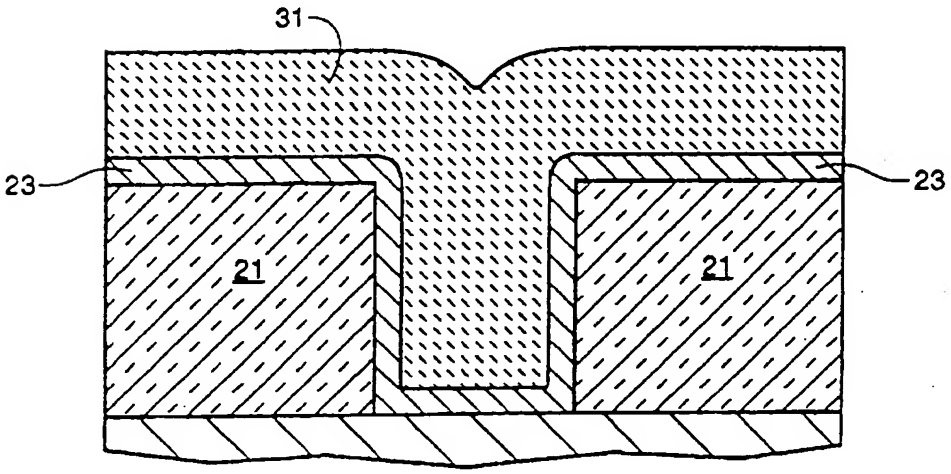


FIG. 3

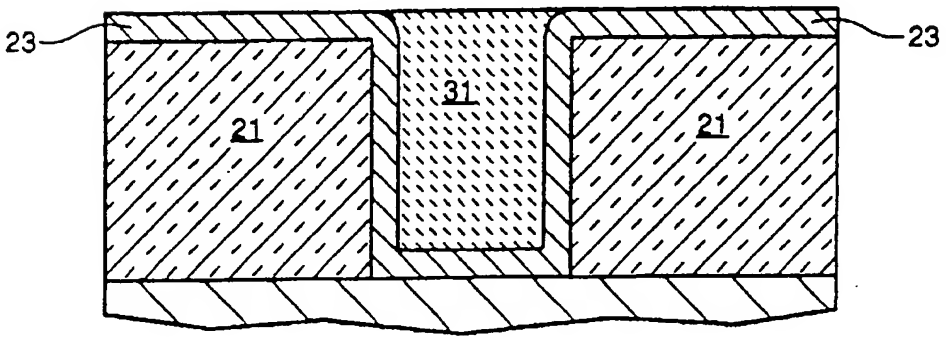


FIG. 4

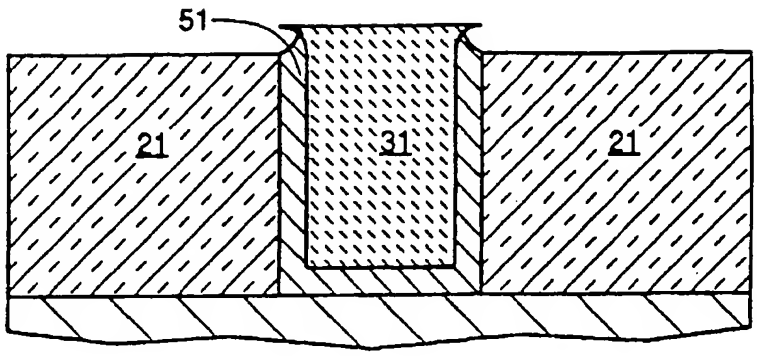


FIG. 5

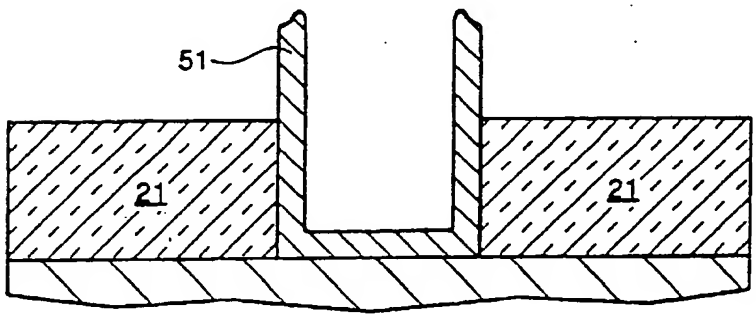


FIG. 6

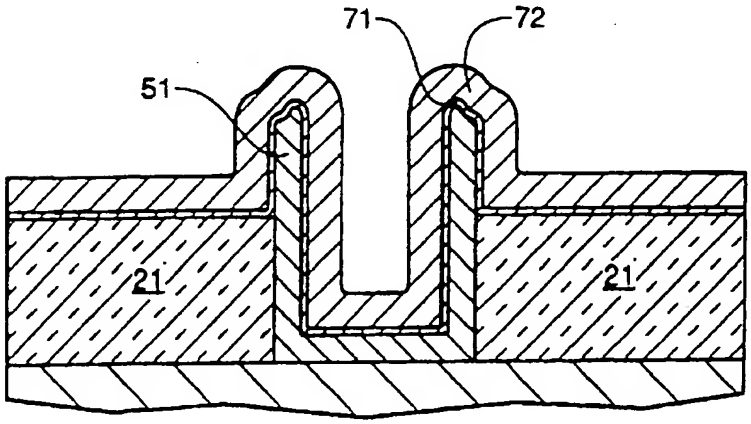


FIG. 7

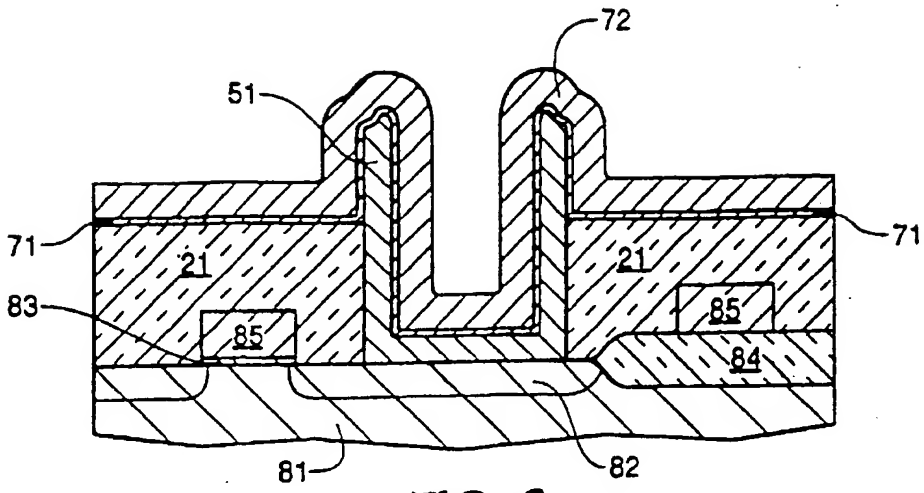


FIG. 8

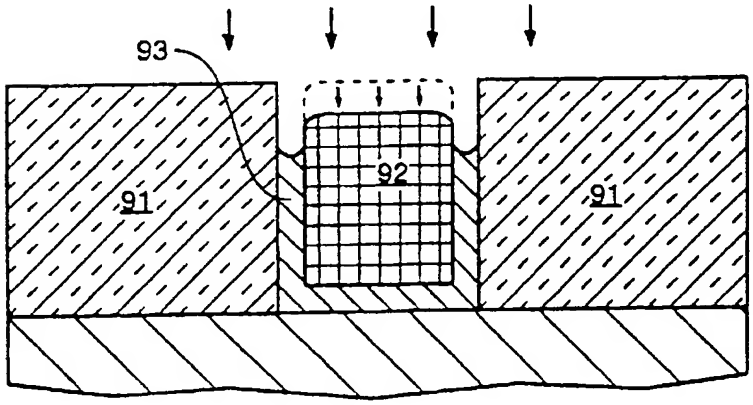


FIG. 9

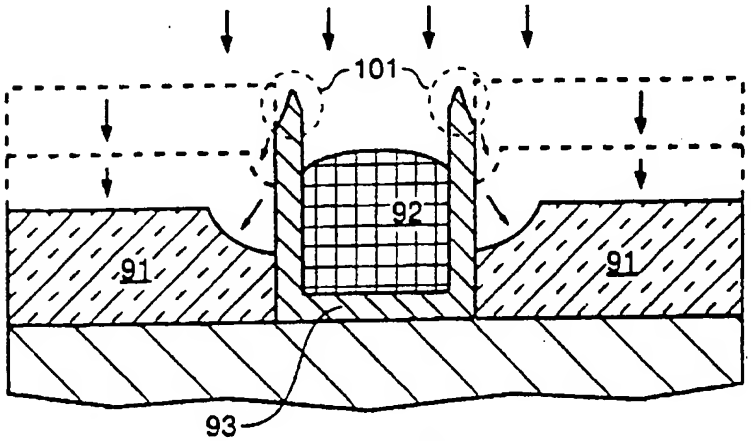


FIG. 10

OPTIMIZED CONTAINER STACKED CAPACITOR DRAM CELL UTILIZING SACRIFICIAL OXIDE DEPOSITION AND CHEMICAL MECHANICAL POLISHING

Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.

CROSS-REFERENCE TO RELATED APPLICATION

This is a continuation to U.S. patent application Ser. No. 07/850,746, filed Mar. 13, 1992, now U.S. Pat. No. 5,162,248.

FIELD OF THE INVENTION

This invention relates to semiconductor circuit memory storage devices and more particularly to a process for fabricating three-dimensional stacked capacitor structures that may be used in such storage devices as high-density dynamic random access memories (DRAMs).

BACKGROUND OF THE INVENTION

In dynamic semiconductor memory storage devices it is essential that storage node capacitor cell plates be large enough to retain an adequate charge or capacitance in spite of parasitic capacitances and noise that may be present during circuit operation. As is the case for most semiconductor integrated circuitry, circuit density is continuing to increase at a fairly constant rate. The issue of maintaining storage node capacitance is particularly important as the density of DRAM arrays continues to increase for future generations of memory devices.

The ability to densely pack storage cells while maintaining required capacitance levels is a crucial requirement of semiconductor manufacturing technologies if future generations of expanded memory array devices are to be successfully manufactured.

One method of maintaining, as well as increasing, storage node size in densely packed memory devices is through the use of "stacked storage cell" design. With this technology, two or more layers of a conductive material such as polycrystalline silicon (polysilicon or poly) are deposited over an access device on a silicon wafer, with dielectric layers sandwiched between each poly layer. A cell constructed in this manner is known as a stacked capacitor cell (STC). Such a cell utilizes the space over the access device for capacitor plates, has a low soft error rate (SER) and may be used in conjunction with inter-plate insulative layers having a high dielectric constant.

However, it is difficult to obtain sufficient storage capacitance with a conventional STC capacitor as the storage electrode area is confined within the limits of its own cell area. Also, maintaining good dielectric breakdown characteristics between poly layers in the STC capacitor becomes a major concern once insulator thickness is appropriately scaled.

A paper submitted by N. Shinmura, et al., entitled "A Stacked Capacitor Cell with Ring Structure," Extended Abstracts of the 22nd International Conference on Solid State Devices and Materials, 1990, pp. 833–836, discusses a 3-dimensional stacked capacitor incorporating a ring structure around the main electrode to effectively double the capacitance of a conventional stacked capacitor.

The ring structure and its development is shown in FIGS. 1(c) through 1(g), pp. 834 of the article mentioned above. FIG. 1(a), on the same page shows a bird's eye-view of storage electrodes. The storage node is formed by two polysilicon layers that form a core electrode encircled by a ring structure. Capacitor dielectric film surrounds the whole surface of the storage node electrode and then is covered with a third polysilicon layer to form the top capacitor electrode and completes the storage cell. This design can be fabricated using current methods and increases storage capacitance by as much as 200%.

Also, [in] a paper submitted by T. Kaga, et al., entitled "Crown-Shaped Stacked-Capacitor Cell for 1.5-V Operation 64-Mb DRAM's," IEEE Transactions on Electron Devices. VOL. 38, NO. 2, February 1991, pp. 255–261, discusses a self-aligned stacked-capacitor cell for 64-Mb DRAM's, called a CROWN cell. The CROWN cell and its development are shown in FIGS. 7(d) through 7(f), pp. 258 of this article. The crown shaped storage electrode is formed over word and bit lines and separated by [a] *an* oxide/nitride insulating layer with the top insulating layer being removed to form the crown shape. Capacitor dielectric film surrounds the whole surface of the storage node electrode and the top capacitor electrode is formed to complete the storage cell.

The present invention develops an existing stacked capacitor fabrication process to construct and optimize a three-dimensional container stacked capacitor cell. The capacitor's bottom plate (or storage node plate) is centered over a buried contact (or node contact) connected to an access transistor's diffusion area. The method presented herein provides fabrication uniformity and repeatability of the three-dimensional container cell.

SUMMARY OF THE INVENTION

The invention is directed to maximizing storage cell surface area in a high density/high volume DRAM (dynamic random access memory) fabrication process. An existing capacitor fabrication process is modified to construct a three-dimensional stacked container capacitor. The capacitor design of the present invention defines a stacked capacitor storage cell that is used in a DRAM process, however it will be evident to one skilled in the art to incorporate these steps into other processes requiring volatile memory cells, such as VRAMs or the like.

After a silicon wafer is prepared using conventional process steps, the present invention develops the container capacitor by etching a contact opening into a low etch rate oxide. The contact opening is used as a form for deposited polysilicon that conforms to the sides of the opening walls. Within the thin poly lining of the oxide container a high etch-rate oxide, such as ozone TEOS, is deposited over the entire structure thereby bridging across the top of the oxide container. The high etch-rate oxide is planarized back to the thin poly by using Chemical Mechanical Polishing (CMP). This CMP step is selective such that oxide is removed with sufficient overetch and stops on the thin poly. The resulting exposed poly is then removed to separate neighboring containers either through an isotropic wet poly etch or an additional CMP with the chemical aspect modified to now etch and selectively remove the poly and not the oxide. The two oxides, having different etch rates, are then etched by a single wet dilute BOE etch step, thereby leaving a free-standing poly container cell, with all the inside (high etch rate) oxide removed, that is equal in height to the depth of the original contact opening. In addition, a pre-determined amount of low etch rate oxide is removed, thereby leaving

oxide surrounding the [,]container, poly for both structural support and process integration for further processing which requires oxide to be left above the word lines.

The present invention uses a higher etch-rate oxide inside the container to block the container poly etch. This high etch rate oxide is completely removed during oxide etch back. This protects the container during processing without adding photoresist and introducing extra processing steps or unwarranted contaminants. A standard CMP oxide etch is utilized that allows fabrication uniformity and repeatability across the wafer which cannot be achieved by resist filled container processes.

Another advantage of filling the container with high etch rate oxide is that the poly can be etched with a low cost, timed wet poly etch, while partially filled containers (as seen in FIG. **9**), due to inherent recession of resist **92** height (to allow for sufficient process margin), will not allow a wet poly etch without loss in cell height **93**, loss in uniformity and repeatability across the wafer's surface. Because this invention can be etched isotropically at poly etch, it avoids the recessing (overetch of the storage poly container **93** in FIG. **9**) and splintering effects caused by a dry etch poly process.

As seen in FIG. **10**, splintering effects **101** of storage node poly **93** result from a dry anisotropic etch (due to non-uniform etching of polycrystalline silicon **93**) because the plasma etch reacts faster along heavily doped grain boundaries. Splinters **101** later tend to 'break off' in subsequent processing leading to contamination particulates. The trenching of the poly leads to the side-walls of the poly container to be exposed, thus making it impossible to wet etch the oxide around the cell without translating the trenched poly horizontal portion of the etch into surrounding oxide **91** thereby leaving a ring of thin oxide around [he] *the* container cell.

The present invention also protects the vertical sidewall of the oxide form by covering it with poly, thereby making a horizontal wet oxide etch back possible. In addition, all films which see etch processing, CMP or otherwise, are subsequently removed thereby acting as sacrificial films such that particles created during the CMP etch do not contaminate the inside of the poly containers.

FIG. **1** shows a gray scale reproduction of a SEM photograph of an array of poly containers **12** which demonstrates the uniformity and repeatability of poly containers **12** across substrate *11* that results from utilizing the process steps of the present invention discussed hereinafter.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a gray-scale reproduction of a SEM (Scanning Electronic Microscope) photograph of a cross-sectional view of an array of container poly rings;

FIG. **2** is a composite cross-sectional view of an in-process wafer portion depicting the beginning steps of the present invention, said steps comprising forming a planarized layer of low etch rate oxide, etching a buried contact and placing a thin layer of conformal poly;

FIG. **3** is a cross-sectional view of the in-process wafer portion of FIG. **2** after formation of a layer of high etch rate oxide;

FIG. **4** is a cross-sectional view of the in-process wafer portion of FIG. **3** after planarization of the high etch rate oxide;

FIG. **5** is a cross-sectional view of the in-process wafer portion of FIG. **4** following a wet etch back of the exposed thin poly layer;

FIG. **6** is a cross-sectional view of the in-process wafer portion of FIG. **5** following an etch of both low etch rate and high etch rate oxides;

FIG. **7** is a cross-sectional view of the in-process wafer portion *of* FIG. **6** following blanket formations of conformal cell dielectric and polysilicon, respectively;

FIG. **8** is a cross-sectional view of a storage cell created by the present invention when integrated into a stacked capacitor fabrication process; [and]

FIG. **9** is a composite cross-sectional view of an in-process wafer portion depicting a container cell filled with photoresist prior to patterning; and

FIG. **10** is a composite cross-sectional view of the in-process wafer portion of FIG. **9** depicting splintering of storage node poly and formation of a thin ring of oxide surrounding the storage node poly following an anisotropic etching to pattern a container cell.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The invention is directed to maximizing storage cell surface area, as well as providing uniform and repeatable, defect free, storage cell structures across a given substrate, in a high density/high volume DRAM fabrication process, in a sequence shown in FIGS. **2–7**.

A silicon wafer is prepared using conventional process steps up to the point of processing an array of storage cell capacitors. Capacitor cell fabrication will now follow.

The storage capacitor of each memory cell will make contact directly to an underlying diffusion area. Each underlying diffusion area will have two storage node connections isolated from a single digit line contact by access transistors formed by poly word lines crossing the active area. Normally each diffusion area within the array is isolated from one another by a thick field oxide. The diffusion areas can be arranged in interdigitated columns and non-interdigitated rows or simply parallel and in line to one another in both the vertical and horizontal directions. As previously mentioned, the diffusion areas are used to form active MOS transistors (serving as access transistors to each individual capacitor) that can be doped as NMOS or PMOS type FETs depending on the desired use.

Referring now to FIG. **2**, a thick layer of low etch rate oxide **21** is formed over an existing topography of a given substrate. Oxide **21** is then planarized, preferably by chemical-mechanical planarization (CMP) techniques down to a predetermined thickness. The thickness of planarized oxide **21** depends on the height that is desired for the poly container structure yet to be formed. The height of the resulting poly structure will determine the capacitor plate surface area that will be required to sufficiently hold a charge. It has been shown that a structure of approximately 1.0–1.5μ is sufficient to construct a reliable 64M DRAM cell using optimized cell dielectric (Container height depends on such factors as container diameter, dielectric constant and thickness of oxides used which are brought to light in the continuing discussion.). A contact opening **22** is then etched into oxide **21** thereby allowing access to the underlying topography (for DRAM-capacitor purposes this opening would normally expose a diffusion region conductively doped into a starting substrate). Contact opening **22** not only allows access to the underlying topography but also provides a form for a subsequent placed layer of thin poly. This thin poly is now formed, preferably by CVD, as a layer of conformal polysilicon **23** and is placed overlying planarized oxide **21**, the patterned edges of oxide **21** and the exposed

underlying topography. Poly **23** may either have been deposited insitu doped or deposited insitu doped and rugged HSG poly for added cell capacitance or it may be subsequently doped.

Referring now to FIG. **3**, a thick layer of oxide **31** having a high etch rate is formed over poly **23**. Oxide **31** is thick enough to completely fill the poly lined contact opening **22**.

Referring now to FIG. **4**, oxide layer **31** is removed down to poly **23**, preferably by CMP which will selectively stop on the first exposed upper regions of poly **23**.

Referring now to FIG. **5**, the exposed upper portions of poly **23** are removed to separate neighboring poly structures, thereby forming individual containers **51** residing in contact openings **22** and exposing underlying oxide **21**. The areas of poly **23** that are removed may be accomplished by performing a poly etch selective to oxide, which could be a timed wet etch or an optimized CMP poly etch. A very significant advantage of this process flow when a CMP etch step is utilized is that the inside of the future container **51** is protected from 'slurry' contamination that is inherent in the CMP step which proves difficult to remove in high aspect ratio storage containers (0.5μ inside diameter by 1.5μ high).

Referring now to FIG. **6**, both oxides **21** and **31**, which have different etch rates, are now exposed. At this point, an oxide etch is performed such that oxide **31** is completely removed from inside container **51** while a portion of oxide **21** remains at the base of container **51** and thereby providing an insulating layer between the underlying topography and subsequent layers. **[A]** *An* etch rate ratio of 2:1 or greater between (a ratio of 4:1 is preferred) oxide **31** and oxide **[22]** *21* provides sufficient process margin to ensure all of high etch rate oxide **31** inside container **51** is removed during the single etch step, while a portion of oxide **[22]** *21* remains to provide adequate insulation from subsequently formed layers.

Referring now to FIG. **7**, when using this structure to form a capacitor storage node plate container **51[and]**, the remaining portion of oxide **21** is coated with a capacitor cell dielectric **71**. **[And, finally]** *Finally* a second conformal poly layer **72** is placed **[to]** *onto* blanket cell dielectric **71** and serves as a common capacitor cell plate to the entire array of containers **51**. From this point on the wafer is completed using conventional fabrication process steps.

FIG. **8** depicts a cross-section of the present invention integrated into a stacked capacitor process on starting substrate **81**. Container **51** connects to diffusion area **82** and thereby serves as a storage node container plate. Diffusion area **82** is accessed by word line **85** (separated by gate insulator **83**) which in turn spans the channel's active area between diffusion areas **82**. The poly of container **51** is doped to the same conductivity type as underlying diffusion region **82** to insure a good ohmic contact.

It is to be understood that although the present invention has been described with reference to a preferred embodiment, various modifications, known to those skilled in the art, may be made to the structures and process steps presented herein without departing from the invention as recited in the several claims appended hereto.

We claim:

1. A process for fabricating a uniform and repeatable conductive container structure on a starting substrate's existing topography, said process comprising the steps of:

a) forming a blanketing first insulating layer, having a first etch rate, over said existing topography;

b) patterning and etching an opening into said first insulating layer, said opening thereby forming a container form;

c) forming a conformal first conductive layer superjacent said first insulating layer and said container form thereby lining said container form;

d) forming a blanketing second insulating layer, having a second etch rate, superjacent said first conductive layer;

e) removing said second insulating layer via chemical mechanical planarization until *an* upper portion of said first conductive layer is exposed;

f) removing said exposed first conductive *layer* upper **[**layer**]** *portion* until underlying said first insulating layer is exposed, thereby **[**separating said first conductive layer into individual said**]** *forming a* conductive **[**containers**]** *container* having inner and outer walls;

g) removing said first and said second insulating layers such that said second insulating layer is completely removed, thereby exposing the entire inner walls of said conductive container and said first insulating layer is partially removed, thereby exposing an upper portion of said outer walls of said conductive container, wherein the partially remaining first insulating layer provides insulation between **[**said**]** underlying substrate topography and subsequently formed layers;

h) forming a third insulating layer superjacent and coextensive *with* said exposed *inner* walls and *an* inner bottom portion of said *conductive* container and said partially remaining first insulating layer; and

i) forming a second conductive layer superjacent and coextensive *with* said third insulating layer.

2. A process as recited in claim **1**, wherein said first insulating layer is planarized prior to said step of patterning and etching an opening into said first insulating layer.

3. A process as recited in claim **1**, wherein said second insulating layer is a sacrificial layer conducive to said chemical mechanical planarization.

4. A process as recited in claim **1**, wherein said first and said second insulating layers are oxides.

5. A process as recited in claim **1**, wherein said first insulating layer etch rate is a lower etch rate than said second insulating layer etch rate.

6. A process as recited in claim **5**, wherein the etch rate ratio between said second insulating layer etch rate and said first insulating layer etch rate is a ratio of 2:1 or greater.

7. A process as recited in claim **5**, wherein the etch rate ratio between said second insulating layer etch rate and said first insulating layer etch rate is a ratio of 4:1.

8. A process as recited in claim **1**, wherein said first and said second conductive layers are doped polysilicon.

9. A process as recited in claim **8**, wherein said doped polysilicon is formed by **[**insitu**]** *in situ* doped chemical vapor deposition.

10. A process as recited in claim **1**, wherein said first, said second and said third insulating layers are formed by chemical vapor deposition.

11. A process for fabricating a uniform and repeatable conductive container structure on a starting substrate's existing topography, said process comprising the steps of:

a) forming a blanketing first insulating layer, having a first etch rate, over said existing topography;

b) patterning and etching an opening into said first insulating layer, said opening thereby forming a container form;

c) forming a conformal first conductive layer superjacent said first insulating layer and said container forms thereby lining said container form;

d) forming a blanketing second insulating layer, having a second etch rate, superjacent said first conductive layer;

e) removing said second insulating layer until *an* upper portion of said first conductive layer is exposed;

f) removing said exposed first conductive *layer* upper [layer] *portion* via chemical mechanical planarization until underlying said first insulating layer is exposed, thereby [separating said first conductive layer into individual said] *forming a* conductive [containers] *container* having inner and outer walls;

g) removing said first and said second insulating layers such that said second insulating layer is completely removed, thereby exposing the entire inner walls of said conductive container and said first insulating layer is partially removed, thereby exposing an upper portion of said outer walls of said conductive container, wherein the partially remaining first insulating layer provides insulation between [said] underlying substrate topography and subsequently formed layers;

h) forming a third insulating layer superjacent and coextensive *with* said exposed *inner* walls and *an* inner bottom portion of said *conductive* container and said partially remaining first insulating layer; and

i) forming a second conductive layer superjacent and coextensive *with* said third insulating layer.

12. A process as recited in claim [1] *11*, wherein said first insulating layer is planarized prior to said step of patterning and etching an opening into said first insulating layer.

13. A process as recited in claim [1] *11*, wherein said second insulating layer is a sacrificial layer that is planarized by chemical mechanical planarization.

14. A process as recited in claim [1] *11*, wherein said first and said second insulating layers are oxides.

15. A process as recited in claim [1] *11*, wherein said first insulating layer etch rate is a lower etch rate than said second insulating layer etch rate.

16. A process as recited in claim **15**, wherein the etch rate ratio between said second insulating layer etch rate and said first insulating layer etch rate is a ratio of 2:1 or greater.

17. A process as recited in claim **15**, wherein the etch rate ratio between said second insulating layer etch rate and said first insulating layer etch rate is a ratio of 4:1.

18. A process as recited in claim **1**, wherein said first and said second conductive layers are doped polysilicon.

19. A process as recited in claim **18**, wherein said doped polysilicon is formed by [insitu] *in situ* doped chemical vapor deposition.

20. A process as recited in claim [1] *11*, wherein said first, said second and said third insulating layers are formed by chemical vapor deposition.

21. A process for fabricating a uniform and repeatable conductive container structure on a starting substrate's existing topography, said process comprising the steps of:

a) forming a blanketing first insulating layer, having a first etch rate, over said existing topography;

b) patterning and etching an opening into said first insulating layer, said opening thereby forming a container form;

c) forming a conformal first conductive layer superjacent said first insulating layer and said container form, thereby lining said container form;

d) forming a blanketing second insulating layer, having a second etch rate, superjacent said first conductive layer;

e) removing said second insulating layer via chemical mechanical planarization until *an* upper portion of said first conductive layer is exposed;

f) removing said exposed first conductive *layer* upper [layer] *portion* via chemical mechanical planarization until underlying said first insulating layer is exposed, thereby [separating said first conductive layer into individual said] *forming a* conductive [containers] *container* having inner and outer walls;

g) removing said first and said second insulating layers such that said second insulating layer is completely removed, thereby exposing [the] entire inner walls of said conductive container and said first insulating layer is partially removed, thereby exposing an upper portion of said outer walls of said conductive container, wherein the partially remaining first insulating layer provides insulation between [said] underlying substrate topography and subsequently formed layers;

h) forming a third insulating layer superjacent and coextensive *with* said exposed *inner* walls and *an* inner bottom portion of said *conductive* container and said partially remaining first insulating layer; and

i) forming a second conductive layer superjacent and coextensive *with* said third insulating layer.

22. A process as recited in claim **21**, wherein said first insulating layer is planarized prior to said step of patterning and etching an opening into said first insulating layer.

23. A process as recited in claim **21**, wherein said second insulating layer is a sacrificial layer conducive to said chemical mechanical planarization.

24. A process as recited in claim **21**, wherein said first and said second insulating layers are oxides.

25. A process as recited in claim **21**, wherein said first insulating layer etch rate is a lower etch rate than said second insulating layer etch rate.

26. A process as recited in claim **25**, wherein the etch rate ratio between said second insulating layer etch rate and said first insulating layer etch rate is a ratio of 2:1 or greater.

27. A process as recited in claim **25**, wherein the etch rate ratio between said second insulating layer etch rate and said first insulating layer etch rate is a ratio [ob] *of* 4:1.

28. A process as recited in claim **21**, wherein said first and said second conductive layers are doped polysilicon.

29. A process as recited in claim **28**, wherein said doped polysilicon is formed by [insitu] *in situ* doped chemical vapor deposition.

30. A process as recited in claim **21**, wherein said first, said second and said third insulating layers are formed by chemical vapor deposition.

31. A process for fabricating a DRAM container storage capacitor on a silicon substrate having active areas, word lines and digit lines, said process comprising the following sequence of steps:

a) forming a blanketing first insulating layer, having a first etch rate, over [said] existing topography;

b) patterning and etching an opening into said first insulating layer, said opening thereby forming a container form;

c) forming a conformal first conductive layer superjacent said first insulating layer and said container form, thereby lining said container form;

d) forming a blanketing second insulating layer, having a second etch rate, superjacent said first conductive layer;

e) removing said second insulating layer via chemical mechanical planarization until *an* upper portion of said first conductive layer is exposed;

f) removing said exposed first conductive *layer* upper [layer] *portion* until underlying said first insulating layer is exposed, thereby [separating said first conductive layer into individual said] *forming a* container storage [capacitors] *capacitor* having inner and outer walls;

g) removing said first and said second insulating layers such that said second insulating layer is completely removed, thereby exposing the entire inner walls of said container storage capacitor and said first insulating layer is partially removed, thereby exposing an upper portion of said outer walls of said container storage capacitor, wherein the partially remaining first insulating layer provides insulation between [said] *an* underlying substrate topography and subsequently formed layers;

h) forming a third insulating layer superjacent and coextensive *with* said exposed *inner* walls and *an* inner bottom portion of said *storage* capacitor and said partially remaining first insulating layer; and

i) forming a second conductive layer superjacent and coextensive *with* said third insulating layer.

32. A process as recited in claim **31**, wherein said first insulating layer is planarized prior to said step of patterning and etching an opening into said first insulating layer.

33. A process as recited in claim **31**, wherein said second insulating layer is a sacrificial layer [conductive] *conducive* to said chemical mechanical planarization.

34. A process as recited in claim **31**, wherein said first and said second insulating layers are oxides.

35. A process as recited in claim **31**, wherein said first insulating layer etch rate is a lower etch rate than said second insulating layer etch rate.

36. A process as recited in claim **35**, wherein the etch rate ratio between said second insulating layer etch rate and said first insulating layer etch rate is a ratio of 2:1 or greater.

37. A process as recited in claim **35**, wherein the etch rate ratio between said second insulating layer etch rate and said first insulating layer etch rate is a ratio of 4:1.

38. A process as recited in claim **31**, wherein said first and said second conductive layers are doped polysilicon.

39. A process as recited in claim **38**, wherein said doped polysilicon is formed by [insitu] *in situ* doped chemical vapor deposition.

40. A process as recited in claim **31**, wherein said first, said second and said third insulating layers are formed by chemical vapor deposition.

41. A process for fabricating a DRAM container storage capacitor on a silicon substrate having active areas, word lines and digit lines, said process comprising the following sequence of steps:

a) forming a blanketing first insulating layer, having a first etch rate, over [said] existing topography;

b) patterning and etching an opening into said first insulating layer, said opening thereby forming a container form;

c) forming a conformal first conductive layer superjacent said first insulating layer and said container form, thereby lining said container form.

d) forming a blanketing second insulating layer, having a second etch rate, superjacent said first conductive layer;

e) removing said second insulating layer until *an* upper portion of said first conductive layer is exposed;

f) removing said exposed first conductive *layer* upper [layer] *portion* via chemical mechanical planarization until underlying said first insulating layer is exposed, thereby [separating said first conductive layer into individual said] *forming a* container storage [capacitors] *capacitor* having inner and outer walls;

g) removing said first and said second insulating layers such that said second insulating layer is completely removed, thereby exposing the entire inner walls of said container storage capacitor and said first insulating layer is partially removed, thereby exposing an upper portion of said outer walls of said container storage capacitor, wherein the partially remaining first insulating layer provides insulation between [said] *an* underlying substrate topography and subsequently formed layers;

h) forming a third insulating layer superjacent and coextensive *with* said exposed *inner* walls and *an* inner bottom portion of said *storage* capacitor and said partially remaining first insulating layer; and

i) forming a second conductive layer superjacent and coextensive *with* said third insulating layer.

42. A process as recited in claim **41**, wherein said first insulating layer is planarized prior to said step of patterning and etching an opening into said first insulating layer.

43. A process as recited in claim **41**, wherein said second insulating layer is a sacrificial layer that is planarized by chemical mechanical planarization.

44. A process as recited in claim **41**, wherein said first and said second insulating layers are oxides.

45. A process as recited in claim **41**, wherein said first insulating layer etch rate is a lower etch rate than said second insulating layer etch rate.

46. A process as recited in claim **45**, wherein the etch rate ratio between said second insulating layer etch rate and said first insulating layer etch rate is a ratio of 2:1 or greater.

47. A process as recited in claim **45**, wherein the etch rate ratio between said second insulating layer etch rate and said first insulating layer etch rate is a ratio of 4:1.

48. A process as recited in claim **41**, wherein said first and said second conductive layers are doped polysilicon.

49. A process as recited in claim **48**, wherein said doped polysilicon is formed by [insitu] *in situ* doped chemical vapor deposition.

50. A process as recited in claim **41**, wherein said first, said second and said third insulating layers are formed by chemical vapor deposition.

51. A process for fabricating a DRAM container storage capacitor on a silicon substrate having active areas, word lines and digit lines, said process comprising the following sequence of steps:

a) forming a blanketing first insulating layer, having a first etch rate, over [said] existing topography;

b) patterning and etching an opening into said first insulating layer, said opening thereby forming a container form;

c) forming a conformal first conductive layer superjacent said first insulating layer and said container form, thereby lining said container form;

d) forming a blanketing second insulating layer, having a second etch rate, superjacent said first conductive layer;

e) removing said second insulating layer via chemical mechanical planarization until *an* upper portion of said first conductive layer is exposed;

f) removing said exposed first conductive *layer* upper [layer] *portion* via chemical mechanical planarization until underlying said first insulating layer is exposed, thereby [separating said first conductive layer into individual said] *forming a* container storage [capacitors] *capacitor* having inner and outer walls;

g) removing said first and said second insulating layers such that said second insulating layer is completely removed, thereby exposing the entire inner walls of said container storage capacitor and said first insulating layer is partially removed, thereby exposing an upper

portion of said outer walls of said container storage capacitor, wherein the partially remaining first insulating layer provides insulation between [said] underlying substrate topography and subsequently formed layers;

h) forming a third insulating layer superjacent and coextensive *with* said exposed *inner* walls and *an* inner bottom portion of said *storage* capacitor and said partially remaining first insulating layer; and

i) forming a second conductive layer superjacent and coextensive *with* said third insulating layer.

52. A process as recited in claim **51**, wherein said first insulating layer is planarized prior to said step of patterning and etching an opening into said first insulating layer.

53. A process as recited in claim **51**, wherein said second insulating layer is a sacrificial layer conducive to said chemical mechanical planarization.

54. A process as recited in claim **51**, wherein said first and said second insulating layers are oxides.

55. A process as recited in claim **51**, wherein said first insulating layer etch rate is a lower etch rate than said second insulating layer etch rate.

56. A process as recited in claim **55**, wherein the etch rate ratio between said second insulating layer etch rate and said first insulating layer etch rate is a ratio of 2:1 or greater.

57. A process as recited in claim **55**, wherein the etch rate ratio between said second insulating layer etch rate and said first insulating layer etch rate is a ratio of 4:1.

58. A process as recited in claim **51**, wherein said first and said second conductive layers are doped polysilicon.

59. A process as recited in claim **58**, wherein said doped polysilicon is formed by [insitu] *in situ* doped chemical vapor deposition.

60. A process as recited in claim **51**, wherein said first, said second and said third insulating layers are formed by chemical vapor deposition.

61. A process for fabricating a capacitor on a substrate, said process comprising the steps of:

providing a first insulating layer on said substrate, said insulating layer having an opening therein forming a container and being subject to a first etch rate;

forming a generally conformal first conductive layer over said first insulating layer and in said container;

forming a second insulating layer above said first conductive layer, wherein said second insulating layer is subject to a second etch rate;

removing at least a portion of said second insulating layer through use of chemical mechanical planarization until an upper portion of said first conductive layer is exposed;

removing at least a portion of an upper portion of said first conductive layer until said first insulating layer is exposed; and

etching said first and second insulating layers such that said second insulating layer is completely removed thereby exposing the entire inner walls of said first conductive layer within said container, and such that said first insulating layer is partially removed.

62. The process of claim 61, further comprising the step of forming a third insulating layer over said inner walls of said first conductive layer within said container.

63. The process of claim 62, further comprising the step of forming a second conductive layer over at least a portion of said third insulating layer.

64. A process for fabricating a DRAM containing storage capacitor on a silicon substrate having an existing topography including active areas, word lines and digit lines, said process comprising the steps of:

providing a first insulating layer having a first etch rate, over said existing topography;

forming an opening into said first insulating layer, said opening thereby forming a container;

forming a conformal first conductive layer over said first insulating layer and said container, thereby lining said container;

forming a second insulating layer having a second etch rate, over said first conductive layer;

removing said second insulating layer through use of chemical mechanical planarization until an upper portion of said first conductive layer is exposed;

removing at least a portion of an upper portion of said first conductive layer until said first insulating layer is exposed, thereby forming a conductive container having inner and outer walls; and

etching said first and second insulating layers such that said second insulating layer is completely removed, thereby exposing the entire inner walls of said first conductive layer within said container, and such that said first insulating layer is partially removed.

65. The process of claim 64, further comprising the step of forming a third insulating layer over said inner walls and an inner bottom portion of said conductive container.

66. The process of claim 65, further comprising the step of forming a second conductive layer over at least a portion of said third insulating layer.

* * * * *

PENDING CLAIMS

Serial No. 10/020,741
TraskBritt Ref. No. 2269-3259.1US
Client Ref. No. 91-0473.02/RE

1-60. (canceled)

61. (currently amended) A process for fabricating a capacitor on a substrate, said process comprising the steps of:

providing a first insulating layer on said substrate, said first insulating layer having an opening therein forming a container;

forming a generally conformal first conductive layer, over said first insulating layer and in said container;

forming a second insulating layer over the entire said first conductive layer; and

removing a portion of said second insulating layer overlying an uppermost portion of portion of said first conductive layer through use of chemical mechanical planarization until said uppermost portion of said first conductive layer is exposed.

62. (original) The process of claim 61, further comprising the step of removing at least a portion of said upper portion of said first conductive layer until said first insulating layer is exposed.

63. (original) The process of claim 61, wherein said second insulating layer is a sacrificial layer conducive to said chemical mechanical planarization.

Exhibit E

64. (original) The process of claim 61, wherein said first and said second insulating layers are oxides.

65. (original) The method of claim 61, wherein said first insulating layer is subject to a first etch rate and said second insulating layer is subject to a second etch rate, and wherein said first etch rate is a lower etch rate than said second etch rate.

66. (currently amended) A process for fabricating a DRAM containing storage capacitor on a silicon substrate having an existing topography including active areas, word lines and digit lines, said process comprising the steps of:

providing a first insulating layer having a first etch rate, over said existing topography;

forming an opening into said first insulating layer, said opening thereby forming a container;

forming a conformal first conductive layer over said first insulating layer and said container, thereby lining said container;

forming a second insulating layer, having a second etch rate, over the entire said first conductive layer; and

removing said second insulating layer through use of chemical mechanical planarization until an uppermost portion of said first conductive layer is exposed.

67. (original) The process of claim 66, further comprising the step of removing at least a portion of said upper portion of said first conductive layer until said first insulating layer is exposed, thereby forming a conductive container having inner and outer walls.

68. (original) The process of claim 66, wherein said second insulating layer is a sacrificial layer conducive to said chemical mechanical planarization.

69. (original) The process of claim 66, wherein said first and said second insulating layers are oxides.

70. (original) The method of claim 66, wherein said first insulating layer etch rate is a lower etch rate than said second insulating layer etch rate.

71. (currently amended) A process for fabricating a DRAM container storage capacitor on a silicon substrate having an existing topography including active areas, word lines and digit lines, said process comprising the steps of:

providing a first insulating layer, having a first etch rate, over said existing topography;

forming an opening into said first insulating layer, said opening thereby forming a container;

forming a conformal first conductive layer over said first insulating layer and said container, thereby lining said container;

forming a second insulating layer, having a second etch rate, over the entire said first conductive layer; and

removing said second insulating layer through use of chemical mechanical planarization until an uppermost portion of said first conductive layer is exposed;

removing at least a portion of said upper portion of said first conductive layer until said first insulating layer is exposed, thereby forming a conductive container having inner and outer walls.

Joseph Walkowski

From: Joseph Walkowski
Sent: Monday, May 02, 2005 10:47 AM
To: 'cdennison@ovonyx.com'
Subject: Micron Reissue Application

Dear Chuck,

Sorry to be a bother, but I am following up on my email below with respect to the Supplemental Reissue Declaration we are required to file with the U.S. patent office to secure issuance of a patent from the pending reissue application. Unfortunately, we are facing a deadline of next Tuesday, May 10th, so I would appreciate receiving back a signed and dated copy of the declaration by facsimile or as an email attachment at your earliest convenience. My prior email and the attachments appear below.

I am also afraid I will be sending you another email today regarding another Micron reissue application where you are an inventor along with Guy Blalock, where we are similarly required to file a Supplemental Reissue Declaration.

Thanks and best regards,

Joe Walkowski
TraskBritt, PC

-----Original Message-----
From: Joseph Walkowski
Sent: Friday, April 01, 2005 3:36 PM
To: 'cdennison@ovonyx.com'
Cc: Debra Mitchell
Subject: Micron Reissue Application

Dear Chuck,

We have straightened out the claim language errors I noted in my email of Novmber 14, 2004 with regard to the pending reissue application, and I am sending you the following for your consideration in deciding whether you are in a position to execute the enclosed Supplemental Reissue Declaration:

1) PDF copy of US Patent 5270241
2) PDF copy of Reissue US Patent 38049
3) Microsoft Word copy of the allowed claims in the pending reissue application Serial No. 10/020,741, which is a continuation of #2. The specification and drawings are the same as in #1 and #2 above, so I am not sending these.

The Supplemental Reissue Declaration is also in Word.

If you would sign the Supplemental Reissue Declaration and fax it back to me at 801-531-9168 or scan it and send it as an email attachment, it would be most appreciated. If you have questions, I will be back in the office on April 7th, and please feel free to call me at 1-800-900-2001 or email me and I will respond upon my return.

Thank you very much for entertaining this request. I sincerely apologize for the imposition. We are just trying to do our job here at the firm.

Please give my best to Lia.

Joe Walkowski


US05270241.pdf (807 KB)


JSRE38049E.pdf (1 MB)


pending claims.doc (33 KB)


Suppl. Reissue Decl.doc (87 KB...

Exhibit F

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Dennison et al.

Serial No.: 10/020,741

Filed: December 12, 2001

For: OPTIMIZED CONTAINER STACKED CAPACITOR DRAM CELL UTILIZING SACRIFICIAL OXIDE DEPOSITION AND CHEMICAL MECHANICAL POLISHING

Confirmation No.: 2283

Examiner: T. Nguyen

Group Art Unit: 2813

Attorney Docket No.: 2269-3259.1US
(91-0473.02/RE)

NOTICE OF EXPRESS MAILING

Express Mail Mailing Label Number: EL994822930US

Date of Deposit with USPS: May 26, 2005

Person making Deposit: Steve Wong

REQUEST FOR TRANSFER OF SURRENDERED ORIGINAL PATENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This request is submitted in response to an action under *Ex parte Quayle* mailed on January 10, 2005.

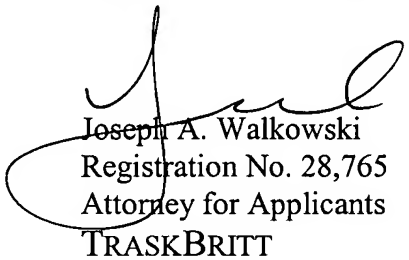
The Office Action requests that the original patent, or a statement as to loss or inaccessibility of the original patent, must be received before this reissue application can be allowed under 37 CFR 1.178.

"An applicant may request that a surrendered original patent be transferred from an abandoned reissue application to a continuation or divisional reissue application." M.P.E.P 1416 (1400-43, Rev. 2, May 2004).

Original U.S. letters patent number 5,270,241 were previously surrendered on October 27, 2000, under Reissue Application No. 08/759,058, now US Patent No. RE38,049 E, issued March 25, 2003. A copy of the date-stamped return postcard is attached evidencing receipt of the original letters patent.

Applicants respectfully request that the previously surrendered originally patent be transferred from the abandoned reissue application to the present continuation reissue application.

Respectfully submitted,



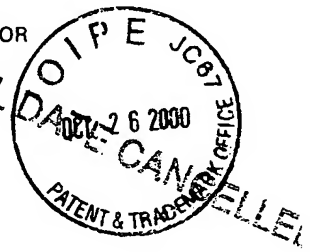
Joseph A. Walkowski
Registration No. 28,765
Attorney for Applicants
TRASKBRITT
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: May 26, 2005
ERC/dlm:dn

Document in ProLaw

THE PATENT / TRADEMARK OFFICE MAILROOM DATE STAMPED HEREON IS AN ACKNOWLEDGEMENT THAT ON THIS DATE THE PATENT & TRADEMARK OFFICE RECEIVED:

Communication Transmittal (in duplicate); Amendment under 37 C.F.R. §1.116 (16 pages); Petition for extension of time (in duplicate); Check No. 14883 in the amount of 110.00 (one month extension); and Original letters patent 5,270,241.



MAIL DATE CANCELLED

Invention:	OPTIMIZING CONTAINER STACKED CAPACITOR DRAM CELL UTILIZING SACRIFICIAL OXIDE DEPOSITION AND CHEMICAL MECHANICAL POLISHING
Applicant(s):	Charles H. Dennison, et al.
Filing Date:	October 7, 1996
Serial No.:	08/759,058
Date Sent:	October 26, 2000 via express mail label no. EL700257093US

Client/Matter Docket No.: 2269/3259US
ERC/le